
Features

- Supports Various Atmel Devices: 16V8, 20V8, 22V10, 750, 750B, F1500A, 2500B, F1508AS, F750C, F1504AS
- Full CUPL Hardware Description Language Using "C"-like Syntax
- Design Entry Includes: Boolean Equations, State Machines, and Truth Tables
- Macros Allow Library Development, and Macro Reusability
- Five-level Logic Minimization Algorithm
- Functional Unit Delay Behavioral Simulator
- Menu Driven Operation

Description

Atmel-WinCUPL is an entry level PLD design system. It offers full design entry, simulation, and JEDEC file generation of Atmel PLDs. Atmel-WinCUPL offers the basic features of Logical Devices' WinCUPL PLD design environment. It is well suited for small PLD design and verification. The package is specifically designed to support development with Atmel Programmable Logic Devices. Atmel-WinCUPL supports: 16V8, 20V8, 22V10, 750, 750B, 750C, 1500, 2500B, 1508, 1504 devices. Support for other manufacturer's PLDs can be added directly from Logical Devices.

Atmel-WinCUPL supports multiple design entry methods. State machine, truth tables and high level Boolean equation can be used. Atmel-WinCUPL also accepts inputs from schematic entry tools and other HDLs.

Multiple logic minimization algorithm are available. Different algorithms will provide different results for each design. Therefore, a user benefits from the availability of multiple algorithms.

A unit delay simulator allows quick design verification. Simulation is the simplest way of checking a design's functionality. An integrated simulator allows quick design iteration.

Once a design is completed, Atmel-WinCUPL generates standard JEDEC files. Device programming is done with these files.

System Requirements

- 486/Pentium-based PC
- 8 MB Memory
- 10 MB Hard Disk Space
- Windows NT/95/98



Atmel-WinCUPL Design Tool for Atmel Programmable Logic Devices

ATDS1000PC





Atmel Headquarters

Corporate Headquarters

2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe

Atmel U.K., Ltd.
Coliseum Business Centre
Riverside Way
Camberley, Surrey GU15 3YL
England
TEL (44) 1276-686-677
FAX (44) 1276-686-697

Asia

Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan

Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs

1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset

Zone Industrielle
13106 Rousset Cedex
France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Fax-on-Demand

North America:
1-(800) 292-8635
International:
1-(408) 441-0732

e-mail

literature@atmel.com

Web Site

<http://www.atmel.com>

BBS

1-(408) 436-4309

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