A.2

ICL

7502

ICL Technical Literature

Control Sheet

Number 80011824
Sheet 1

Terminal Controller 7502 : Technical Description

ISSUE	No OF SHEETS	AFFECTED SHEETS AND ALTERATIONS	DESIGN AUTHORITY	CED	TECHNICAL LITERATURE DEPARTMENT	ECN	DATE
1	78	PROVISIONAL ISSUE			RPBell		19.9.74

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TABLES

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ILLUSTRATIONS

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RELATED DOCUMENTS

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Terminal Controller 7502 : Technical Diagrams	80011825
Terminal Controller 7502 : Engineers Facilities	80014264
Terminal Controller 7502 : Servicing Procedures	80011821
Logic Diagram Set	845111nn
Engineers Test Unit Logic Diagram Set	847064nn
Configurator	80014028
Teleload Flowcharts	80012976
Teleload Procedures	80012977
Video Keystation 7560, 7561 : Technical Description	80011826
Termiprinter : Technical Description	81803311

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Number 80011824
Sheet 10

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1 INTRODUCTION

The basic Terminal Controller 7502 consists of a Processor, Store and Input/Output coupler. Other units may be fitted as detailed in this description to extend the facilities provided by the controller (see System Description section 4).

The controller is tested using an Engineers Test Unit (ETU) which is described in document 80014264.

Also for use by the engineer is a store PCB (P009) containing a number of engineering tests. This PCB is described in document 80014264.

Reference to the Technical Diagram Set 80011825 is made in the form TD sheet n. x.

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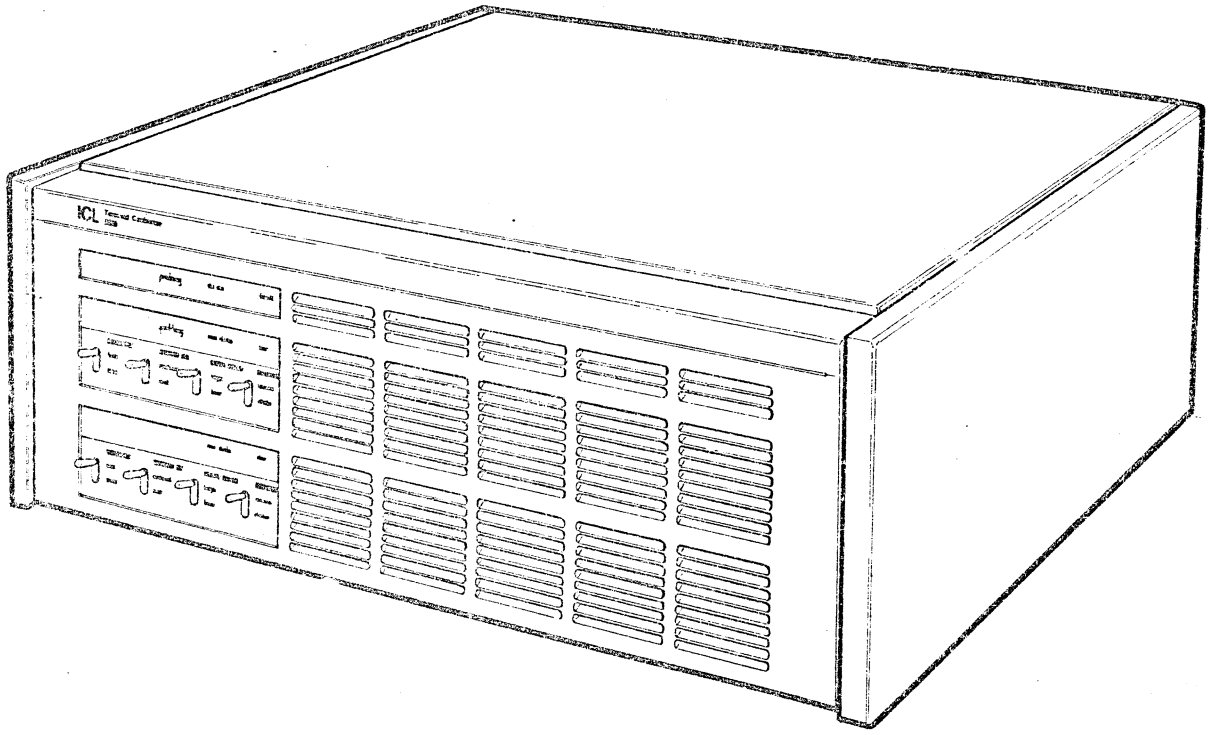
Front



TERMINAL CONTROLLER 7502

2 CONSTRUCTION (see TD section 1)

The Terminal Controller is housed in a welded steel cabinet. A light aluminium cladding is then fitted over the outside of this cabinet.

The power supply is located in the rear portion of the cabinet. Access to the power supply and backplane is gained by removing the outer cladding from the cabinet and then swinging the power supply up out of the cabinet (see Servicing Procedures 80011821).

A fan is used to cool the equipment and is an integral part of the power supply assembly.

A replaceable air filter is located behind the equipment front panel.

The PCBs used in this equipment are 'double height Macro boards' which are inserted horizontally into the equipment. The board positions in the backplane are numbered one to nine, starting at the top. Permissable board positions are given in table 2.1.

Note: Position one is a half width position for future highway extension purposes and thus cannot be used as a PCB position.

PCB Type No.	Description	Permissible positions
P001	Processor	2,3
P002 or P010	Program Store	Anywhere
P003	Display Coupler	4,5,6,7
P004	I/O Coupler	8,9
P005 *	ETU Coupler	2,3

*See Engineers Maintenance Manual 80014264

TABLE 2.1 PERMISSABLE PCB POSITIONS

All input/output connections to the controller are by sockets located at the rear of the equipment.

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3 OPERATORS CONTROL PANEL

3.1 Introduction

All the components of the Operators Control Panel are mounted on a single PCB type 5141 which is located at the left hand side of the Terminal Controller behind the facia panel.

Controls for operating two Modems are included but at present only the top set are used.

3.2 Indicator Lamps

The indicator lamps are light emmitting diodes (LEDs) driven by single transistor amplifiers. Their indication and driving source are detailed in table 3.1.

Lamp	Function	Driving Source
d. c. on	Indicates that d. c. power is available.	+5V and 0V power rails to PCB 5141
polling	Illuminated when Terminal Controller is transmitting data to Modem.	PCB P004 (see section 12)
dsr	Illuminated when Modem has switched transmission line to Terminal Controller	PCB P004 (see section 12)
rec data	Illuminated when data is being received from Modem	PCB P004 (see section 12)
fault	Illuminated during first four seconds of power up and when a hardware detected fault exists	PCB P001 Watch dog Timer (see section 6.14)

TABLE 3.1 LAMP INDICATIONS

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3.3 Switches

The switches control the modes of operation and match the Terminal Controller to the Modem in use. The switch settings are defined in table 3.2.

Switch Settings				Modem/Mode
DATASET	STANDBY	DATARATE	DUPLEX	
voice	not	high	full	Talk Through/Modem loop back test
voice	not	high	half	
voice	not	low	full	
voice	not	low	half	
voice	standby	high	full	
voice	standby	high	half	
voice	standby	low	full	
voice	standby	low	half	
data	not	high	full	Modem 7, Point to Point. 4 Wire.
data	not	high	half	Modem 7, Point to Point. 2 Wire or 4 Wire Multidrop.
data	not	low	full	Modem 7, Point to Point. 4 Wire.
data	not	low	half	Modem 7, Point to Point. 2 Wire or 4 Wire Multidrop.
data	standby	high	full	Not used.
data	standby	high	half	Modem 7 Standby/ Modem 1 1200 baud
data	standby	low	full	Not used
data	standby	low	half	Modem 7 Standby/ Modem 1 600 baud.

TABLE 3.2 SWITCH SETTINGS

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4 SYSTEM DESCRIPTION

To be issued

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5 HIGHWAY

5.1 Introduction

The highway comprises interface lines as defined in table 5.1 and TD sheet 2.1. For details of the highway timing see TD sheets 6.1 to 6.5.

Name of Line	Signal Name	Number of Lines	Source
Store Address	STORE ADDR	22	Lines 2^0-2^{15} - Processor Lines 2^{16}-2^{21} Store Expansion Module
Data Output	DOUT	16	Processor
Data Input	DIN	16	Processor
Device Address	DEV ADD	6	Processor
Clock Lines	10.752 MHz TP1 TP2 TP3	1 1 1 1	Processor
Store Strobe	STORE STR	1	Processor
Device Strobe	DEV STR	1	Processor
Hold	HOLD	1	Store or Device
General Reset	GEN RES	1	Timer (Processor)
Transfer Acceptable	TRAN ACC	1	Device
State 2^1	STATE 2^1	1	Processor
Store Write L.S byte	WRITE LSB	1	Processor
Store Write MS byte	WRITE MSB	1	Processor
Store Read Protect	READ PROTECT	1	Store
Store Write Protect	WRITE PROTECT	1	Store
Access Demand	ACCESS DEM	1	DMA Control
Access Enable	ACC EN	1	Processor
Service Request	SER REQ	1	Device
Double Byte	DOUBLE BYTE	1	Device

TABLE 5.1 HIGHWAY INTERFACE LINES

5.2 Store Address

The Store Address is carried on the 22 Store Address Lines. In minimum systems only lines 2^0 to 2^{15} are signficant with lines 2^{16} to 2^{22} permanently 'high'. In enhanced systems lines 2^{16} to 2^{21} are provided by a Store Expansion Module (see section) but the address thus provided is one preloaded into the module by a preceding instruction sequence.

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5.3 Data Output Lines

During store transfers data to the store is carried on these lines. During device transfers these same lines carry data and (or) control information to the addressed device. It therefore follows that store and device transfers cannot take place at the same time.

5.4 Data Input Lines

During store transfers provided Store Strobe (see section 5.8)is'true' data from the addressed store location is placed on the Data Input lines. During device transfers, provided Device Strobe (see section 5.9) is true and the controlling command is either Read Data or Read Control, the addressed device places either data or Status information on the Data Input lines.

5.5 Device Address

The six Device Address lines are used to access one of the 64 basic device ports. When sub-addressing is used (see section 12.11) the Store Address lines 2^8 to 2^{15} are used to access the sub-port within the addressed basic port.

5.6 Device Commands

The Store Address lines 2^6 and 2^7 carry the Device Commands as defined in table 5.2.

Store Address Lines		Command
2^7	2^6	
0	0	Read Data
0	1	Write Data
1	0	Read Control
1	1	Write Control

TABLE 5.2 DEVICE COMMANDS

5.7 Clock Lines

Four clock lines are provided for basic timing throughout the equipment and are defined in TD sheet 6.1.

5.8 Store Strobe

The Store Strobe is set whenever a store transfer is to be performed. The timing of the strobe and other related lines is defined in TD sheets 6.2 and 6.3.

5.9 Device Strobe

The Device Strobe is set whenever a device transfer is to be performed. The timing of the strobe and other related lines is defined in TD sheets 6.4 and 6.5.

5.10 Hold

When the Hold line is set the time available for a store or device transfer is extended. The highway timing related to the Hold line is defined in TD sheets 6.3 and 6.5. If the relevant strobe disappears before the end of Hold then Hold will be cleared within 100ns of the back edge of the strobe.

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5.11 General Reset

When the General Reset line is 'set' all the machine software is reset to a Start routine and all current transfers are terminated. The line is 'set' for approximately four seconds on 'power-up' and for at least 1.6m seconds in the event of a Timer Service Request not being honoured within 1.66ms.

5.12 Transfer Acceptable

This line is 'set' during device transfers to signify that the current transfer is satisfactory and that no other type of transfer was expected by the addressed device instead of the one that was used. The timing related to the Transfer Acceptable line is detailed in TD sheets 6.4 and 6.5.

5.13 State 2^1

This line is 'set when the processor is in machine state S_2 or S_3 (non supervisor states).

5.14 Store Write L.S Byte and Store Write M.S Byte

These two lines are store write enable lines. They may be set independantly so only one byte of data (8 bits) may be written to store if required. The timing of these lines is detailed in TD sheets 6.2 and 6.3.

5.15 Store Read Enable and Store Write Enable

These lines are used in conjunction with preset links in the store to identify 4K byte sections of store as being 'privileged access' or general access. When Read Enable is set general access to that store block is allowed for read operations and similarly when Write Enable is set general access is allowed for write operations. When these lines are not 'Set' an access to the store from states S_2 or S_3 will cause a 'Program Exception' interrupt. The timing related to these lines is defined in TD sheets 6.2 and 6.3.

5.16 Access Demand and Access Enable

These two lines are used by the Direct Memory Access control system to interrupt the processor when direct memory functions are being performed. The Access Demand line runs into the processor from the Direct Memory Access control, and Access Enable runs in the reverse direction. Whenever the DMA control requires access to the highway it sets Access Demand. As soon as the processor has completed its current job on the highway Access Enable is set to indicate that the DMA control is now responsible for the highway.

All processor generated lines with the exception of the Clock lines, Device Address and Access Enable are surrendered to the DMA control. When the DMA control has finished using the highway Access Demand is cleared and the processor regains control clearing Access Enable as it does so. The Direct Memory Access control will clear its influence on the highway within 100ns of loss of Access Enable, while the processor will not influence the surrendered lines beyond 100ns after the front edge of Access Enable.

When the Access Demand is for a transfer as a result of a recognised service request, the Access Demand line must be true within 100ns of the Service request signal to prevent processor service of that service request.

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5.17 Service Request

This line is used to notify the processor (or any other servicing mechanism) that a particular device requires attention. The line must be set within 100ns of a valid address being recognised on the Device Address lines and must be cleared within 100ns of that address being changed.

5.18 Double Byte

This signal is used to indicate that a particular device supports a double byte transfer (word transfer) in place of the normal right justified single byte transfer for the particular transfer being performed. This signal is issued not more than 100ns after the occurance of the device address, sub-address and command. The line is independant of device strobe. The signal is removed within 100ns of the valid conditions being discontinued.

The Double Byte signal is used only for transfers via Direct Memory Access control. The processor does not use this signal.

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6 PROCESSOR

6.1 Introduction

The Terminal Controller processor is contained on a single PCB P001 (842978nn) which is normally located in position 02 in the machine frame. The processor works on a fixed 16 bit word length and all data and instruction paths within the processor utilize a single full 16 bit word.

A number of highway lines as detailed in section 5 table 5.1 are generated in the processor.

6.2 Order Code

The Order Code is described in section 7 and instruction/processor flowcharts are in TD section 3.

6.3 Instruction Register (See TD sheets 2.2, 3.1 and 4.2 reference B1/2)

The 16 bit instruction register is divided into a number of sections:

(a) Bits 12 to 15 form the FN portion of the instruction word and define the current instruction being executed (i.e. 0 - F).

(b) Bits 8 to 11 form the R_1 portion.

(c) Bits 4 to 7 form the R_2 portion.

(d) Bits 0 to 3 form the R_3 portion.

The R_2 portion of the instruction word is derived from one of two registers in the instruction register. One register is the same as the registers containing the other portions of the instruction word and is therefore an ordinary parallel in/parallel out register. When the R_2 portion of the instruction word is derived from this register it is designated R_2+. The second register is countable (i.e. data may be counted up or down after being loaded). When the R_2 portion of the instruction word is derived from this register it is designated $R_2\neq$.

The 16 DIN lines (Data in) are buffered and then applied directly to the instruction register. The data on these lines is loaded into the non-countable sections of the instruction register on the negative going edge of µSCLKHELD (see section 6.9) provided I/P to I is true (see section 6.7).

The data on DIN lines 4 to 7 is loaded into the countable portion of the instruction register when F1 is true i.e. µSCKHELD with either LOADI' or IP to I or (LOAD I'X and $\overline{\text{Instruction register output } 2^2}$) are true.

The contents of the register are counted one place on the positive going edge of the trigger input provided F1 is not true. The count is up when COUNT UP is true and down when COUNT UP is not true.

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6.4 Scratch Pads (See TD sheets 3.2 and 4.2 reference G/H 2/3) (Also refer to section 6.6)

The processor utilizes two scratchpads as immediate working store. Each scratchpad consists of 16 words of the 16 bit RAM storage.

The scratchpads are addressed by various portions of the instruction word, multiplexors which are controlled by the microprogram (see section 6.7) being used to pick off the particular portion of the instruction word required at a particular instance.

For unfrozen (normal) processor operations the two scratchpads hold identical information. For 'interrupt' processing one scratchpad (scratchpad 2) is preserved so that the interrupted program can be saved without loss of information and the program returned to after the interrupt has been cleared.

The 16 registers are referred to by their hexadecimal address 0 to 9 and A to F. All registers except register F (see section 6.4.1) may be freely used in processor operations.

The Address Enable and Write Enable lines control the scratchpads as detailed in table 6.1 (see also section 6.7).

Action	Address Enable	Write Enable	Data Input	Data Output	Comment
Write	0	0	X	$\overline{X}$	Stores input data
Read	0	1	-	$\overline{Y}$	Outputs contents of addressed register
Transparent	1	0	X	$\overline{X}$	Does not store
Disabled	1	1	X	-	Data is not stored and does not appear at output

TABLE 6.1 SCRATCHPAD CONTROL

6.4.1 Register F Bits 2^0 to 2^{13} of register F are used to store the address of the current instruction. The register is incremented by one after each instruction execution unless the current instruction indicates a different procedure.

The two most significant bits 2^{14} and 2^{15} of register F are used to hold the mill status from the last executed arithmetic or logic instruction.

Bits		Status
2^{15}	2^{14}	
0	0	Mill status zero
0	1	Mill status not zero and not negative
1	0	Not Allowed
1	1	Mill status not zero and negative.

TABLE 6.2 MILL STATUS

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During store addressing using register F the two most significant bits of the output address will always be zero independently of the state of 2^{14} and 2^{15} in register F.

6.5 Mill (See TD sheets 2.2 and 4.2 reference J1)

The addressed scratchpad register (see section 6.4) is output directly to the Mill where arithmetic and logical functions are carried out under the control of the microprogram (see table 6.3).

M (H)	S_3 (L)	S_2 (L)	S_1 (L)	S_0 (L)	Function
0	0	0	0	0	$K - \overline{CI}$
0	1	0	0	1	K - L -CI
0	1	1	1	1	K + CI
1	0	0	0	0	K
1	0	0	0	1	KvL
1	0	1	0	1	L
1	0	1	1	0	$\overline{K \neq L}$
1	1	0	0	1	$K \neq L$
1	1	0	1	0	$\overline{L}$
1	1	1	1	0	$\overline{KvL}$
1	1	1	1	1	$\overline{K}$

TABLE 6.3 MILL FUNCTIONS

The outputs from the mill with ACCEN not true (see section 6.10) form the 16 Address lines STORE ADDR 0-15 (see section 5.2).

The mill outputs are also connected to a 2:1 multiplexor where under the control of the microprogram (see section 6.7.9) either the data on these lines or the data on the DIN lines is passed to the inputs to the Q register.

6.6 Q Register (See TD sheets 2.2 and 4.2 reference J5)

The Q register is a 16 bit serial/parallel shift register the output of which with ACCEN not true (see section 6.10) gives the 16 DOUT lines (see section 5.3). It is used as a Mill working register. The output of the Q register is also connected back to the data inputs of the scratchpad, (see section 6.4) thus it can be seen that the scratchpad, provided it is enabled and clocked, stores the contents of the Q register.

Provided Q SHIFT is not true (see section 6.7.10) data at the input to the Q register (lines 2^0 - 2^{15}) is loaded on the negative transition of the L input and appears at the output of the register. When Q SHIFT is true data on the D input to the Q register (i.e. either the most or least significant output bit from the Q register) is loaded at the negative transition of the S input and appears on the register output 2^{15}. At the same time the original contents of the register are shifted down one bit. This provides an arithmetic or cyclic shift operation.

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When INH Q MS is true (see section 6.7.11) the clock to the register containing the most significant byte is inhibited. The preceding description then only applies to the Q register containing the least significant byte.

6.7 Microprogram (See TD sheets 4.2 and 5.1 to 5.3)

The controlling microprogram is held in 10 four-bit Read only Memory (ROM) chips. The starting point of each microprogram sequence is defined by the FN portion of the instruction word (see section 6.7.3). The microprogram outputs are defined in the following sections.

6.7.1 M and S_{0-3} Controls the mill as defined in section 6.5.

6.7.2 CN is applied to the CI input of the mill operating on the least significant byte of the scratchpad output.

6.7.3 FND and INH FND As long as INH FND is true the 2:1 Multiplexor TD sheet 4.2 reference B6 routes bits 0-3 of the microprogram output NμSADDR to the input of the microstep address register. Similarly, when both FND and INH FND are not true. When FND is true and INH FND is not true the four most significant bits (12-15) of the output from the instruction register (see section 6.3) form bits 0-3 of the input to the microstep address register.

6.7.4 F INST is used in two places

(a) as one bit in addressing the condition code ROM (see section 6.8)

(b) to address and enable a ROM which superimposes data on the M, S0-3 and CN outputs of the microprogram ROMs during instructions F, 5 and unfrozen C.

FINST	CINST	
0	0	Normal Mill operation
0	1	C instruction operation
1	0	F instruction operation
1	1	5 instruction operation

TABLE 6.4 FINST OPERATION

Note: Signal CINST is derived from INH QMS and QSHIFT both set.

6.7.5 Access Required (ACC REQ) is used in conjunction with the highway line ACCESS DEM to set logic which controls the access to the highway when a Direct Memory Access unit is in use.

6.7.6 Microprogram Device Strobe (μPDEVST) controls DEV STR (Device Strobe) as defined in TD sheets 6.4, 6.5 and 6.7.

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6.7.7 Microprogram Store Strobe (μPSTSTR) controls STORE STR (Store Strobe) as defined in TD sheets 6.2, 6.3 and 6.8.

6.7.8 Microprogram Store Write (μPSTWRITE) controls the ST WRITE (Store Write) lines as defined in TD sheets 6.2, 6.3 and 6.9.

6.7.9 Input to Q (I/P to Q) controls the 2:1 multiplexor described in section 6.5 routing data to the Q register as detailed in table 6.5.

I/P to Q	Data Routed to Q Register
0	Output from Mill
1	Highway lines DIN 0-15

TABLE 6.5 INPUT TO THE Q REGISTER

6.7.10 Q SHIFT controls the mode of operation (i.e. serial or parallel shift) of the Q register as described in section 6.6. Q SHIFT also enables the trigger on the countable portion of the instruction register as described in section 6.3.

6.7.11 INH Q MS inhibits the most significant byte of the Q register as described in section 6.6 and at the same time enables the write enable line of the least significant byte of scratchpad 2.

6.7.12 Input to Instruction Register (I/P to I) controls the input to the instruction register as described in section 6.3.

6.7.13 Scratchpad Address Enable (SPE1 and SPE2) enables the Address Enable lines of the two scratchpads (SPE1 for scratchpad 1 and SPE2 for scratchpad 2) (see also section 6.4).

6.7.14 Scratchpad Write Enable (SPW1 and SPW2) enables the Write Enable lines of the two scratchpads (SPW1 for scratchpad 1 and SPW2 for Scratchpad 2) (see also section 6.4).

6.7.15 SP1ADD0, 1 controls the multiplexor TD sheet 4.2 reference D2 and thus controls the address source for scratchpad 1 as detailed in table 6.6.

ADDRESS LINE 1	ADDRESS LINE 0	
0	0	Instruction Register output bits 4 to 7 from the non-countable register form address.
0	1	Instruction Register output bits 8 to 11 form scratchpad address.
1	0	Scratchpad 2 address used to address scratchpad 1.
1	1	Addresses register F

TABLE 6.6 SCRATCH PAD 1 ADDRESS DECODE

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6.7.16 SP2 ADD0, 1 controls the multiplexor TD sheet 4.2 reference D3 and thus controls the address source for scratchpad 2 as detailed in table 6.7.

ADDRESS LINE 1	ADDRESS LINE 0	
0	0	Scratchpad 1 address used to address scratchpad 2.
0	1	Instruction register output bits 0-3 used as address.
1	0	Address derived from countable portion of instruction register (bits 4-7)
1	1	Address derived from ETU.

TABLE 6.7 SCRATCHPAD 2 ADDRESS DECODE

6.7.17 Conditions (CC 2^3 to 2^0) The conditions outputs are applied to a decoder (TD sheet 4.2 reference D5) where the lines are decoded as detailed in table 6.8.

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Address	Signal	Action
0	Null	Processor action not affected.
1	L4	Enables logic TD sheets 4.2 ref E2 such that instruction register outputs 0-3 are superimposed on scratchpad 2 outputs 0-3. Also disables Address lines 14 and 15. See also address 5.
2	DISF2W	Disables the Store Write lines during the Frozen 2 instruction.
3	L8s	Enables logic TD sheet 4.2 ref E1 such that instruction register outputs 0-7 are superimposed on scratchpad 2 outputs 0-7 and at the same time instruction register output 7 is superimposed on scratchpad 2 outputs 8-15.
4	L12 s	Enables logic TD sheet 4.2 ref E1 such that instruction register outputs 0-11 are superimposed on scratchpad 2 outputs 0-11. At the same time instruction register output 11 is superimposed on scratchpad 2 output 12-15.
5	CONC	Controls a 2:1 multiplexor which directs the condition codes (see section 6.8) onto the mill output lines 14 and 15 in place of these lines. Address 1 (L4) also has this effect. This signal also disables the Store Write lines and substitutes Instruction register bits 0 and 1 for scratchpad 2 address lines 0 and 1.
6	LOAD I'	Trailing edge of μSCLKHELD causes DIN lines 4 to 7 to be loaded into the countable portion of the instruction register.
7	LOAD I'X	Trailing edge of μSCLKHELD and instruction register output 2 False causes DIN lines 4 to 7 to be loaded into the countable portion of the instruction register.
8	COUNT UP	Causes the countable portion of the instruction register to count as described in section 6.3.
9	L_8	Enables logic TD sheet 4.2 ref E_1 such that instruction register outputs 0-7 are superimposed on scratchpad 2 outputs 0-7.
A	KEYS	Enables Address lines 14 and 15 and signals to the ETU to place the word set up on the data keys onto the DIN Highway.
B	R_3*	Inverts bit 0 of scratchpad 2 address.
C	L3	Disables Address lines 14 and 15 and at the same time enable logic TD sheet 4.2 ref E2 such that instruction register outputs 0-3 are superimposed on scratchpad 2 outputs 0-3.
D	SET HALF WORD	Disables the Write Enable lines to the most significant byte of the scratchpad thus only the least significant byte may be written to. (See also section 6.4.)
E	SET STATE	Causes the machine state S_0 - S_3 to be set. (See section 6.13.)
F	Not used.	

TABLE 6.8 CONDITIONS DECODE

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6.7.18 BRANCH 2^3 to 2^0 controls two 8:1 multiplexors the output from either of which can cause a jump in the microprogram as detailed in table 6.9

Branch Address	Conditions for Jump
0	Microprogram not affected : No jump.
1	Instruction Register output bit 2 logic 1
2	Instruction Register output bit 3 logic 1
3	Instruction Register output bit 5 logic 1
4	Instruction Register output bit 6 logic 1
5	Instruction Register output bit 11 logic 1
6	Processor in machine state S1 (see section 6.13)
7	Stop command from ETU (Logic 0)
8	Scratchpad 2 output bit 15 is logic 1
9	Output bits 0 to 2 of countable portion of Instruction Register are 0.
A	Output of countable portion of Instruction Register is F.
B	Highway line TRAN ACC (Transfer Acceptable true).
C	Condition Code output CC0 true (logic 1)
D	Condition Code is such that the output from ROM12 is logic 1 (see TD sheet 5.5).
E	Scratchpad 1 address does not equal F.
F	Not used.

TABLE 6.9 BRANCH DECODE

6.7.19 UNFREEZE Unfreezes the processor and causes the microprogram to revert to the unfrozen portion.

6.7.20 Next Microstep address (NμsADD0-5) is fed back to the address lines of the microprogram ROMs via a multiplexor and six-bit register and thus determines the next microstep. (See section 6.7.2 for a description of the multiplexor control.)

6.8 Mill Condition Codes

The Condition Codes decode table is held in a 256 bit ROM (64x4) (see TD sheet 4.2 references E5 and sheet 5.4). Bits 0 and 1 of the Condition Codes are passed to a 2 bit parallel in/parallel out register and thus to one set of inputs of a 2:1 multiplexor (TD sheet 4.2 reference H4). Bits 14 and 15 of the Mill output (see section 6.5) are applied to the second set of multiplexor inputs. When CONC (Concatinate) is not true (see table 6.8) the Mill outputs 14 and 15 are passed to the multiplexor controlling the input to the Q register (see sections 6.5 and 6.7.9). When CONC is true the Condition Code bits 0 and 1 are substituted for Mill outputs 14 and 15.

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All four Condition Code outputs 0-3 are also used to address and 2nd ROM which generates SKIP (see TD sheet 4.2 reference F5 and sheet 5.5).

6.9 Machine Timing and Strobes

All the machine timing signals and strobes are derived from a 10.752MHz crystal controlled oscillator located on the Processor PCB. (See TD sheet 4.3 reference C1.) The oscillator output forms one highway line (see section 5.1) and is also applied to the input of a divide by 'seven Johnson Counter' which gives the highway lines TP1, TP2 and TP3 (see TD sheet 4.3 reference D1 and sheet 6.1). The Strobes, microprogram control lines and Store Write lines are derived from TP1, TP2 and TP3 as detailed in TD sheets 6.6 to 6.9.

6.10 Highway Access (see TD sheet 4.3)

The highway access is controlled by two lines Access Required from the processor microprogram and Access Demand from the DMA (Direct Memory Access, see section). The logic works on the principle of first come first served and is described by means of timing diagrams in TD sheets 6.10 and 6.11.

6.11 Service Request Scanner (see TD sheet 4.4 and section 6.14)

The service request counter (TD sheet 4.4 reference D4) is triggered on the back edge of each μSTEPCLK provided ACCESS DEM or μPDEVST are not true i.e. provided that DMA does not require the highway and provided a Device Transfer is not currently taking place. The output from the counter is placed on the DEV ADD (Device Address) lines and at the same time applied to the input of a six-bit latch. When a device requires service and recognises its own address it raises the Service Request line which then 'sets' the Service Request D-Type (TD sheet 4.4 reference C3). (Unless the DMA indicates control of this device by raising ACC DEM) This in turn latches the device address in the six-bit latch. The service request counter keeps running and each time a device requires service and recognises its address it raises the Service Request line although only the first address is latched into the six-bit latch. When the counter reaches 3F and μPDEVST is true SEC A STAT is true and thus allows the latched device address on to the DEV ADD lines to check if the Service Request is still pending. If not SEC A STAT true resets the Service Request D Type and unlatches the six-bit latch and the scanner continues looking for service requests starting at address 00.

When the processor examines the Service Request Scanner to determine the address of the device which raised Service Request it does so by means of a Device Transfer instruction. Bits 4 and 5 of the instruction word are 'set' with μPDEVST which then allows the contents of the eight-bit latch on to the DIN lines 0-5. At the same time the above conditions 'set' SR SCAN ADD which 'resets' the Device Strobe D-Type and thus inhibits Device Strobe. SR SCAN ADD 'true' also 'sets' SEC ASTAT which thus allows the contents of the six-bit latch onto the DEV ADD lines. This action confirms that the Service Request still exists and signals this to the program by setting TRANACC on the highway. If the Service Request does not still exist the Service Request D-Type is reset.

During Device Transfers other than to the Service Request Scanner the Mill outputs 0-5 are placed on the DEV ADD lines and thus give the Device Address to which the transfer is destined.

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6.12 Interrupts

When the processor is in an interruptable machine state (see section 6.13) a Service Request gives rise to an Interrupt at the end of the current instruction cycle (see TD sheet 4.4 reference H3 and FS section 2). The machine is switched to State 4 and scratchpad 2 preserved. Processing then resumes at location 0000_{16} with the processor in the non-interruptable state S4. Scratchpad 2 is then unfrozen. Once the interrupting service request has been processed the program is restarted at the point of interruption following the recovery of the scratchpad contents from the main store.

A program exception interrupt is also included (see TD sheet 4.4 reference H3) which is used when operating in certain machine states (see section 6.13) to provide protection to the store contents and to the machines I/O system. This interrupt routine is entered in the same way as the I/O interrupts and at the same time the Store Write lines are inhibited (see TD sheet 4.3 reference G5).

6.13 Machine States (see TD sheet 4.4)

The processor has five states identified as S0, S_1 S_2, S_3 and S_4. States S0 to S3 are defined by the instruction register output bits 0 and 1 along with microprogram output SET STATE (see table 6.10). State S4 is set directly from the microprogram. The machine state S0 to S3 is held in two D-Types (TD sheet 4.4 reference D2 and D4) and is latched into a two-bit latch when the machine enters state S4. The contents of the two-bit latch are placed on DIN lines 6 and 7 at the same time as the device address is placed on DIN lines 0-5 (see section 6.11) i.e. when interrupt processing.

Instruction Bits 1	0	Machine State
0	0	S0
0	1	S_1
1	0	S_2
1	1	S_3

TABLE 6.10 MACHINE STATES

6.13.1 S0 State This is the non-interruptable state. In this state all processor instructions are available to the program, and the presence of a service request (which would cause an interrupt from an interruptable state) can be interrogated under program control. This state is used for programmed input/output control, and for supervisory work within the software structure.

6.13.2 S1 State This is an interruptable state. Its properties are as for State S0 except that the program controlled service request interrogation will normally not operate, as the service request causes a reversion to state S4 and an entry into the interrupt processing routine (see section 6.12). This state is used for processing store maintenance and update jobs, which may be interrupted for I/O work.

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6.13.3 S2 State This is a semi- interruptable state. In this state the program controlled I/O instructions and access to store sections, which are designated as protected stores, will cause a program exception interrupt to occur. In this state any I/O service request will be withheld for 160μs after which the processor will switch automatically into State S3. The instructions for changing processor state are restricted to changing between states S2 and S3 only. This state is used to allow untested I/O software to be evaluated.

6.13.4 S3 State This is an interruptable state. Its properties are as for state S2 except that I/O service requests will cause an immediate interrupt to occur. This state is used for evaluation of non trusted store maintenance routines.

6.13.5 S4 State is the same as state S0 but uses a different Order Code (see section 7.6 and TD section 3).

6.14 Watch-dog Timer (see TD sheet 4.3)

The Watch-dog Timer is designated device address 00 and every 3.3ms sets a Service Request which is serviced by a Write Control transfer.

A timer service request that is outstanding for more than 1.6ms causes a system GENRES forcing the processor to revert to state S4 and the program to skip to location 0001. This is interpretted by the software as an irrecoverable crash condition requiring a complete reload/restart. The timer stop when the processor is stopped using the engineers STOP key or the INH W-DOG key.

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7 ORDER CODES

7.1 Introduction

Each instruction in the Order Code occupies a single sixteen-bit word which causes the processor to operate as detailed in the flowcharts in TD section 3.

When the processor is in Machine States S_0, S_1, S_2 and S_3 (see section 6.13) the Normal Order Code is used (see section 7.2).

When the processor is in Machine State S_4 certain instructions in the Normal Order Code are replaced by alternative instructions (see section 7.6).

7.2 Normal Order Code (Machine States 0, 1, 2 and 3)

The processor Normal Order Code may be conveniently divided into three sections:

(a) Register Manipulation in which only the processor is affected (see section 7.3).

(b) Control sequence modifications which permit the normal sequential execution of instructions to be modified (see section 7.4).

(c) Store or Input/Output operations which allow the processor to alter conditions external to itself (see section 7.5).

7.3 Register Manipulation (Normal Order Code)

7.3.1 Shift Right (FUNCTION 3)

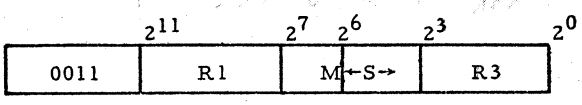

FIGURE 7.1 '3' INSTRUCTION WORD

This instruction shifts a copy of the contents of the register addressed by R3, S plus 1 places to the right, and writes the result into the register addressed by R1. If M is set to zero, bits lost from the right hand end of the word are reintroduced at the left hand end, i.e. a cyclic shift. If M is set to one, the sign bit (2^{15}) is reintroduced at the left hand end of the word, i.e. an arithmetic shift.

7.3.2 Load Immediate (FUNCTION 6)

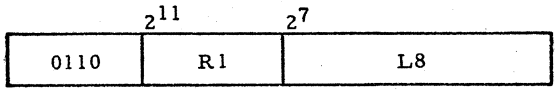

FIGURE 7.2 '6' INSTRUCTION WORD

This instruction loads the least significant (right hand) byte of the register addressed by R1 with the literal L8, and clears the most significant byte to zeros.

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7.3.3 Add Immediate (FUNCTION 8)

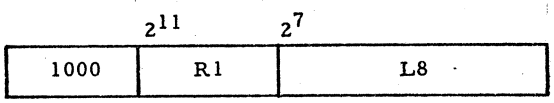

FIGURE 7.3 '8' INSTRUCTION WORD

This instruction takes the literal L8 which is sign extended to form a complete 16 bit word which is then added into the register addressed by R1.

7.3.4 And Immediate (FUNCTION 9)

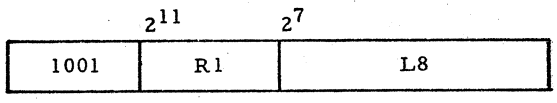

FIGURE 7.4 '9' INSTRUCTION WORDS

This instruction takes the least significant eight bits of itself (L8) and logically AND's this byte into the least significant eight bits of the register addressed by R1. The most significant eight bits of the register are set to zero.

7.3.5 Register-Register Functions (FUNCTION F)

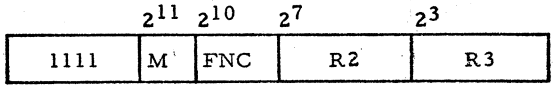

FIGURE 7.5 'F' INSTRUCTION WORDS

This instruction performs operations on the contents of the register addressed by R2 using the data in the register addressed by R3; the result is placed in the register addressed by R2. The contents of the register addressed by R3 are not changed (unless R2 = R3). FNC defines the function as detailed in table 7.1.

2^{10}	2^{9}	2^{8}	Function
0	0	0	'OR'
0	0	1	'AND'
0	1	0	ONES COMPLEMENT
0	1	1	COPY (R3 into R2)
1	0	0	ADD
1	0	1	SUBTRACT
1	1	0	NAND
1	1	1	EXCLUSIVE OR

TABLE 7.1 REGISTER-REGISTER FUNCTIONS

If M equals one, the entire word is used. If M equals zero the least significant byte only is affected, (there is no carry over to the most significant byte). If R2 equals F the M bit will be treated as equal to one irrespective of its actual value.

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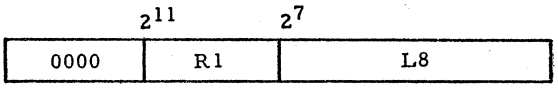
7.4 Control Sequence Modification (Normal Order Code)

7.4.1 Mask Immediate (FUNCTION 0)

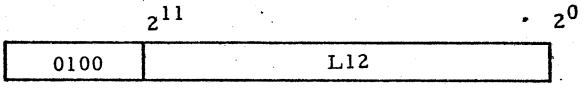


skip if R1 ∧ L8 ≠ 0

FIGURE 7.6 '0' INSTRUCTION WORD

This instruction tests the least significant eight bits of the contents of the register addressed by R1 under the mask of the least significant eight bits of the instruction (L8). The coincidence of any 'one' bit in corresponding position in the register and L8 will cause the next instruction in the sequence to be skipped and the instruction following it to be executed. Lack of such coincidence causes the instruction to function as a 'null' operation.

7.4.2 Jump (FUNCTION 4)



→ PC + L12

FIGURE 7.7 '4' INSTRUCTION WORD

This instruction takes the least significant twelve bits of itself (L12), sign extends these twelve bits to a complete word (by setting each bit 2^{12} to 2^{15} equal to 2^{11}) and adds this word into register F. The new contents of register F form the next instruction address. (The incrementing of register F by one is ommitted once immediately following the execution of a jump instruction.)

7.4.3 Branch On Condition (FUNCTION 5)

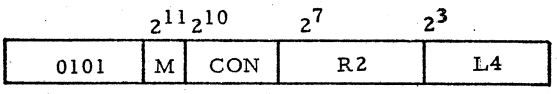


FIGURE 7.8 '5' INSTRUCTION WORD (M = 0)

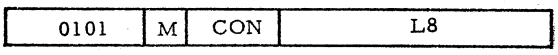


FIGURE 7.9 '5' INSTRUCTION WORD (M = 1)

This instruction causes a branch or jump to occur dependant upon either the conditions within the mill or the presence of a Service Request. The conditions are defined by the CON field of the instruction as detailed in table 7.2.

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CON 2^{10}	CON 2^{9}	CON 2^{8}	Branch Condition
0	0	0	Service Request present
0	0	1	Always branch
0	1	0	Mill Status negative
0	1	1	Mill Status not negative
1	0	0	Mill Status zero
1	0	1	Mill Status not zero
1	1	0	Mill Status not positive
1	1	1	Mill Status positive

TABLE 7.2 BRANCH CONDITIONS (5 INSTRUCTION)

If the selected condition is false, the instruction is treated as a NULL and the next instruction in sequence is executed. If the condition is true, the next instruction address is derived as follows:

If M is set to zero, the four bit unsigned literal (L4) is added to a copy of the contents of the register addressed by R2, the result is loaded into register F and taken as the address of the next instruction. The mill status bits in register F are left unchanged by this branch operation. The incrementing of register F is suppressed once, immediately following the generation of this new address.

If M is set to one, the least significant eight bits of the instruction are signed extended to a complete word, which is added into register F. The new contents of register F are the address of the next instruction. The incrementing of register F is suppressed once immediately following the generation of this new address.

7.4.4 Compare Immediate (FUNCTION 7)

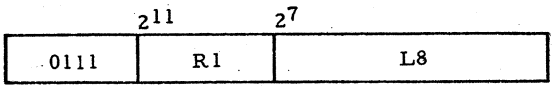

FIGURE 7.10 '7' INSTRUCTION WORD

This instruction tests the contents of the register addressed by R1 and skips the next instruction in sequence if either of the following conditions exists:

(a) If the most significant eight bits of the register are not all zero.

(b) If the least significant eight bits of the register differ from the least significant eight bits of the instruction (L8).

If no skip occurs the instruction function as 'null' operation. When the most significant byte is zero and the least significant byte equals L8 in the register addressed by R1, the instruction is treated as a NULL.

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7.5 Store and Input/Output Operations (Normal Order Code)

7.5.1 Device Transfer (FUNCTION 1)

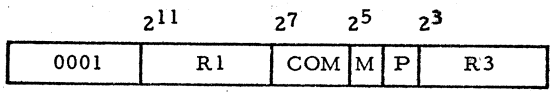

FIGURE 7.11 '1' INSTRUCTION WORD (M=1)

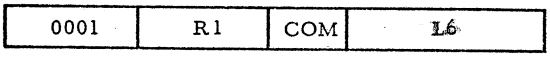

FIGURE 7.12 '1' INSTRUCTION WORD (M=0)

This instruction transfers a single word between an I/O port and the register addressed by R1. The control bits (COM) in the instruction identify the direction of transfer and also determine the function being used within the I/O system by signalling this command over the I/O highway (see table 7.3).

Store Address Lines		Command
2^7	2^6	
0	0	Read Data
0	1	Write Data
1	0	Read Control
1	1	Write Control

TABLE 7.3 I/O COMMANDS

If the M bit is zero, the literal L6 is used to address the I/O port which is being manipulated.

Note: Since the M bit forms part of this literal it is possible to address directly only the 32 lowest numbered ports out of the 64 permitted addresses.

If the M bit is one, and the P bit is zero the contents of the register addressed by R3 are used to supply the I/O port address. Bits 2^0 to 2^5 of the register give the Port Address, bits 2^8 to 2^{15} give the optional Sub-Port Address.

During each device transfer an I/O port may signal that the transfer is acceptable (i.e. the command was the one that I/O port expected). If the transfer is satisfactory the next instruction in sequence is skipped. Attempting to access a non existant I/O port will always result in an unsatisfactory transfer being signalled.

If M and P are both set to one a Read Data Transfer or a Read Control Transfer will transfer the contents of the service request register to the register addressed by R1. This enables the program to identify the cause of an interrupt or to locate an outstanding service request. If a service request is outstanding the next instruction is skipped. A Read Data Transfer will load the register addressed by R1 with the following data:

bits 2^0 to 2^5 - Service Request Address (if request pending)
bits 2^6 and 2^7 - Current Machine State if in State 0 or 1. Previous state if in State 4.
bits 2^8 to 2^{15} - zero

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A Read Control Transfer will give the same result except that Machine State 4 will be selected after instruction execution. A transfer acceptable condition indicates that the service request address is a valid and current address. An unacceptable transfer condition indicates that there is no identified outstanding service request.

7.5.2 Store Transfer (FUNCTION 2) NORMAL

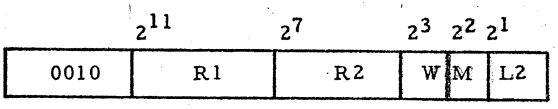

FIGURE 7.13 '2' INSTRUCTION WORD

This instruction transfers a single word between the register addressed by R1 and a specified store location. If W equals zero the transfer is from store to register. If W equals one the transfer is from register to store.

When M equals zero the specified store location is identified by adding the two bit Literal L2 to the contents of the register addressed by R2.

When M equals one, the specified store location is identified by adding to the contents of the register addressed by R2 the contents of a register addressed by a concatinated address field.

The concatinated address field is obtained by replacing the least significant two bits 2^4 and 2^5 of R2 by the unsigned Literal L2.

7.5.3 Dump/Recover Move Register (FUNCTION A)

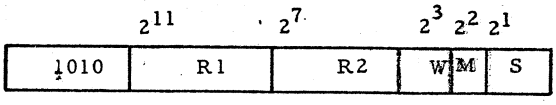

FIGURE 7.14 'A' INSTRUCTION WORD

This instruction is used for storing and reloading the contents of the scratch pad and is used to allow multiple programs to be interleaved. Registers are transferred sequentially stating at a specified register and continuing through ascending addresses until register F has been transferred. The contents of the register addressed by R1 point to the beginning of the 'dump area' in the main store. The dump area starts at the specified location, which contains a control parameter and continues through successive locations (of increasing addresses) each of which holds copies of the contents of successive registers in the scratchpad.

When W equals one the contents of the scratchpad are written into the store. When W equals zero the scratchpad is reloaded from store. In the latter case, since Register F is reloaded, control is handed to the newly loaded program. Register F is incremented by two before the next instruction is fetched, which means that one instruction in sequence is skipped between a dump and the entry on an associated recovery.

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For M equals one, the address of the first register transferred is R2. For M equals zero, the bits 2^4 to 2^7 of the control parameter, to which register R1 is pointing, are used as the first register address.

On completion of the instruction (either storing or recovering), the processor switches into the state defined by the S field of the instruction. State 4 cannot exist at the end of the instruction unless an interrupt occurs.

If the initial state is state 2 or 3 the 2^1 bit of the instruction will be assumed to be one, i.e. state 2 or 3 only can be selected if the initial state is State 2 or 3.

7.5.4 Move Block (FUNCTION B)

NORMAL

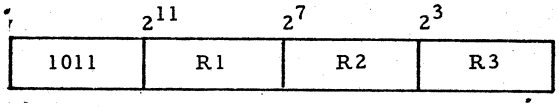

FIGURE 7.15 'B' INSTRUCTION WORD

A copy of the contents of a store location, identified by adding copies of the contents of registers addressed by R1 and R3 is written into the location identified by adding copies of the contents of registers addressed by R2 and R3.

The contents of registers addressed by R3 are examined, and if negative the contents are incremented by one, if positive the contents are decremented by one. If the new contents are not all ones (minus one) the cycle repeats. If the new contents are all ones the instruction is complete. The instruction is interruptable at the end of any cycle. Re-entry to the same instruction will cause continuation of the interrupted operation.

7.5.5 Search Block (FUNCTION C)

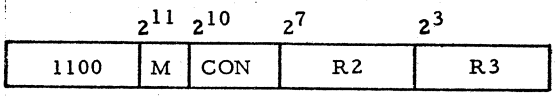

FIGURE 7.16 'C' INSTRUCTION WORD

A store location is addressed by adding copies of the contents of registers addressed by R2 and R3. A register is selected by taking the second register in the even/odd register pair of which the register addressed by R3 is a member (e.g. Register 2 is selected if R3 equals 3).

The selected register is compared with the accessed store location according to the test condition defined by the CON field: see table 7.4.

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CON 2^{10}	CON 2^9	CON 2^8	Test True When:
0	0	0	1s in Register masked with 0s in store
0	0	1	0s in register masked with 1s in store
0	1	0	Register < Store
0	1	1	Register ≮ Store
1	0	0	Register = Store
1	0	1	Register ≠ Store
1	1	0	Register ≯ Store
1	1	1	Register > Store

TABLE 7.4 SEARCH BLOCK TEST CONDITIONS

If M equals one, the register and store are treated as a single sixteen bit word. If M equals zero, the register and store are treated as holding two separate bytes.

When a test true condition is found, the instruction terminates and the next instruction in sequence is skipped. If no test true condition occurs the instruction cycles interruptably with the register addressed by R3 being amended as described in section 7.5.4.

7.5.6 Modify Block (FUNCTION D)

NORMAL

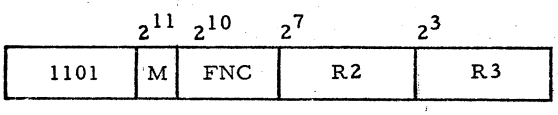

FIGURE 7.17 'D' INSTRUCTION WORD

A store location is addressed by adding copies of the contents of registers addressed by R2 and R3. A register is selected by taking the second register in the even/odd register pair of which R3 is a member (e.g. Register 2 is selected if R3 equals 3).

The FNC field defines the arithmetic or logic function to be performed between the accessed store location, and the selected register, see table 7.5.

2^{10}	2^9	2^8	Operation
0	0	0	OR register with store location
0	0	1	AND register with store location
0	1	0	ONES COMPLIMENT store location
0	1	1	LOAD with most significant byte of register (Least significant byte is unaltered)
1	0	0	ADD register and store location
1	0	1	SUBTRACT store location from register
1	1	0	NAND register with store location
1	1	1	EXCLUSIVE OR register with store location

TABLE 7.5 MODIFY BLOCK FUNCTIONS

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When M equals one the accessed store is modified to hold the value generated as a result of the FNC field. When M equals zero the selected register is modified to hold the value generated as a result of the FNC field.

The instruction cycles interruptably with register R3 being incremented as described in section 7.5.4. Note if M equals zero, the register R3 is always decremented. This permits a full 64K words of store to be 'sumchecked' with one instruction.

7.5.7 Translate Block (FUNCTION E) NORMAL

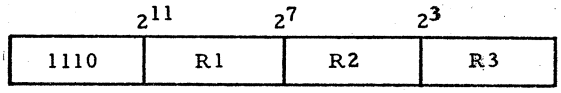

FIGURE 7.18 'E' INSTRUCTION WORD

A store location is addressed by adding together copies of the contents of the registers addressed by R2 and R3. If the register addressed by R3 is negative, only the least significant byte of the store location is altered. If the register R3 is not negative, both bytes are translated individually. Each original byte from the store is treated as a positive displacement (in the range 0-255) which is applied to the base address in the register addressed by R1. A translation table of 256 words is held in store commencing at the base address. The least significant byte only, of each word in the table, is used. The instruction cycles interruptably with the register addressed by R3 being counted as described in section 7.5.4.

7.6 Interrupt Processing Order Code (State 4)

Whenever the processor enters machine State 4 certain instructions in the Store and Input/Output section of the Normal Order code are replaced by the alternative instructions defined in sections 7.7 to 7.9.

7.7 Register Manipulation (Interrupt Processing Order Code)

During interrupt processing all the instructions defined in section 7.3 plus the instructions defined in sections 7.7.1 and 7.7.2 are available.

7.7.1 Access Scratchpad 2 (FUNCTION B) FROZEN

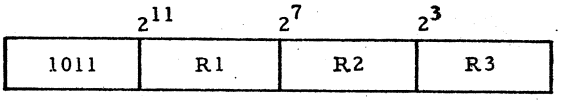

TABLE 7.19 'B' INSTRUCTION WORD [Interrupt Processing]

This instruction is used to access or modify registers saved during an interrupt. The Scratchpad 2 register addressed by R2 is copied into the Scratchpad 1 register addressed by R1. The Scratchpad 2 register is then reloaded from the Scratchpad 1 register addressed by R3. If R1 equals R3 the Scratchpad 2 register is unchanged.

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7.7.2 Load Most Significant Byte (FUNCTION E)

FROZEN

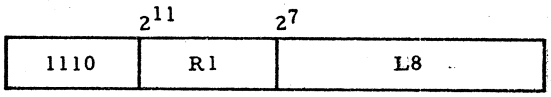

FIGURE 7.20 'E' INSTRUCTION WORD [Interrupt Processing]

This instruction takes the eight-bit Literal L8 and Exclusively OR's it into the most significant byte of the register addressed by R1. The least significant byte of that register is unaltered.

7.8 Control Sequence Modification (Interrupt Processing Order Code)

During interrupt processing all the instructions defined in section 7.4 plus the instruction defined in section 7.8.1 are available.

7.8.1 Execute (FUNCTION D)

FROZEN

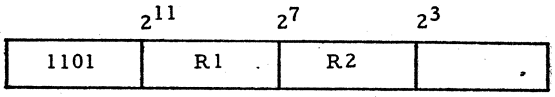

FIGURE 7.21 'D' INSTRUCTION WORD [Interrupt Processing]

The execute instruction allows a single instruction, generated in the register addressed by R1, to be written into the Random Access Memory Store at any point. This instruction is executed as though it was actually in the store location occupied by the execute instruction which invoked it. This permits a program existing in Read Only Memory Store to execute a self generated instruction. The Random Access Memory location used is indicated by the register addressed by R2. If no storage exists at the specified address a NULL instruction is performed.

7.9 Store and Input/Output Operations (Interrupt Processing)

During interrupt processing the instruction defined in section 7.5.1 plus the instructions defined in sections 7.9.1 to 7.9.3 are available.

7.9.1 Store Transfer (FUNCTION 2)

FROZEN

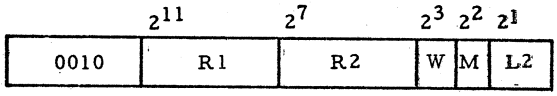

FIGURE 7.22 '2' INSTRUCTION WORD [Interrupt Processing]

This instruction is used to access the interrupted instruction in the event of a program exception interrupt (protection) occurring.

When M equals zero, this instruction is as defined in section 7.5.2 (M=0).

When M equals one, the store address is taken from the Scratchpad 2 register addressed by R2. No displacement is permitted and the L2 field is ignored.

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7.9.2 Move Register (FUNCTION A)

FROZEN

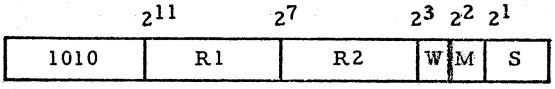

FIGURE 2.23 'A' INSTRUCTION WORD [Interrupt Processing]

If W equals one, this instructions is as defined in section 7.5.3.

When W equals zero, the instruction reloads Scratchpad 1 from Scratchpad 2. Apart from this change the operation is as defined in section 7.5.3. If M equals zero the control parameter is still fetched from store although the transfer is between scratchpads.

7.9.3 Incremental Access (FUNCTION C)

FROZEN

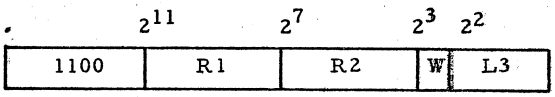

FIGURE 7.24 'C' INSTRUCTION WORD [Interrupt Processing]

This instruction increments by one the contents of the store location addressed by the contents of the store location addressed by the contents of the register addressed by R2. The new contents of this location are then loaded into the register addressed by R2. A second auto indexed address is now obtained by adding the three-bit Literal L3 to a copy of the register addressed by R2.

If W equals zero, the register addressed by R1 is loaded with a copy of the contents of the store location so addressed.

If W equals one, the contents of the register addressed by R1 are copied to the store location so addressed.

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Sheet 7-12

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8 MAIN STORE (8K byte RAM)

8.1 Introduction

This store contains 8K byte of static MOS Random Access Memory (RAM) storage and up to 1252 byte of Read Only Memory (ROM). The ROM storage is divided into two sections. One section contains 1K byte of fixed program routines (described in document 80012977); the other section contains up to 64 words of a Bootstrap routine and Interrupt Entry routines described in document 80012977). The second section is located in the bottom 64 store locations. Store maps and coding charts for the Teleload ROM's are in TD sheets 5.6 to 5.8 and an overall logic diagram of the complete store is in TD sheet 4.5.

8.2 Store Addressing

The store address is carried to the store on the highway lines ADD0-21 which gives a possible 4M word address range of which this store requires a 6K word range. This is selected by means of links as detailed on the overall logic diagrams and in the configurator 80014028. Address lines 0 to 10 are used to address the store chips in blocks of 2K words within the 6K word range of addresses selected by means of the links.

8.3 Hold

As this store does not operate at sufficient speed to complete a cycle in one processor μstep time the highway HOLD line is used to effectively slow down the processor when carrying out RAM store transfers (see TD sheets 6.2 and 6.3).

When Store Strobe is not true the code 1010 is loaded into a four bit down counter (TD sheet 4.5 reference C4). When Store Strobe is true the counter counts down on each positive going edge of the 10.752 MHz clock. At the same time, provided the store address applies to one of the RAM blocks, a 1 is strobed (by the front edge of Store Strobe) into the D-type (TD sheet 4.5 reference E5) and thus gives HOLD. When the four bit counter reaches a count of 0000 the CI output goes true and thus 'resets' the D-type which in turn resets the HOLD line and allows Store Strobe to finish as detailed in the processor description.

8.4 Teleload ROM

The Teleload ROM contains a number of fixed program routines which are described in document 80012977. The ROM data is held on two separate bytes with different location addresses as detailed in TD sheets 5.7 and 5.8. When the most significant output from the four bit counter (see section 8.3) is one, the least significant byte of data is read out of the ROM and passed to the eight bit latch and hence to the DIN lines 0-7. This data also appears on DIN lines 8 to 15 at this time. When the most significant output from the four bit counter is zero, the least significant byte of data is latched in the eight bit latch and the most significant byte of data read out from the ROM. This data is then placed on DIN lines 8-15 and the latch output placed on DIN lines 0-7 thus giving a full word of data.

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8.5 Bootstrap ROMs

Up to 64 words of ROM which can contain a Bootstrap routine will be fitted to the store. It is mandatory that the bottom four words of ROM containing Interrupt Entry routines be used. If more ROM locations are required a further 28 words are available in the ROMs fitted and a further 32 words can be fitted if required. The Bootstrap routine is described in 80012977.

A link is set (TD sheet 4.5 reference E3) such that in one position the Bootstrap ROM replaces the bottom 64 words of RAM. If the Teleload ROM is not fitted then the second link position allows the bottom 64 locations of the Teleload ROM addresses to be filled by the Bootstrap ROM. When the link is in the second position the Bootstrap ROM still replaces the bottom 64 words of RAM.

Tables 8.1 to 8.3 give the store map coding for the bottom four locations of the Bootstrap ROM.

Store Address	Program
0000	2FF2
0001	2FF2
0002	0802
0003	3E3A

TABLE 8.1 BOOTSTRAP ROM: INTERRUPT ENTRY ROUTINES

Address	Coding
0000	0 0 0 0 1 1 0 1
0001	0 0 0 0 1 1 0 1
0002	1 1 1 1 1 1 0 1
0003	1 1 0 0 0 1 0 1

TABLE 8.2 BOOTSTRAP ROM CODING: LS BYTE [Bottom Four Words]

Address	Coding
0000	1 1 0 1 0 0 0 0
0001	1 1 0 1 0 0 0 0
0002	1 1 1 1 0 1 1 1
0002	1 1 0 0 0 0 0 1

TABLE 8.3 BOOTSTRAP ROM CODING: MS BYTE [Bottom Four Words]

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9 MAIN STORE (12K byte RAM)

9.1 Introduction

This store contains 12K byte of static MOS Random Access Memory (RAM) storage and 1K byte of Read Only Memory (ROM). The ROM contains a number of fixed program routines which are described in document 80012977. A map of the ROM is in TD sheets 5.6 to 5.8 and an overall logic diagram of the complete store is in TD sheet 4.6.

9.2 Store Addressing

The store address is carried to the store on the highway lines ADD 0 to 17. Lines 18 to 21 are not used by this store and any one of these lines going true will disable the store completely (see TD sheet 4.6 reference B1). The address lines 0 to 17 give a possible 64K word address range of which this store requires an 8K word range. This is selected by means of links as detailed on the overall logic diagram and in the configurator 80014028. Address lines 0 to 10 are used to address the store chips in blocks of 2K words within the 8K word range of addresses selected by means of the links.

9.3 Hold

As this store does not operate fast enough to complete a cycle in one processor μstep time the highway HOLD line is used to effectively slow down the processor when carrying out store transfers (see TD sheets 6.2 and 6.3).

When Store Strobe is not true the code 0101 is loaded into a four bit up counter (TD sheets 4.6 reference C4). When Store Strobe is true the counter counts up on each positive going edge of the 10.752 MHz clock. At the same time Store Strobe true 'resets' the bistable (TD sheet 4.6 reference C5) which, provided SEL is true, gives HOLD. SEL is true provided the store is addressed by a valid address. When the four bit counter reaches a count of 1111 the CI output goes true and this 'sets' the bistable which in turn resets the HOLD line and allows the Store Strobe to finish as detailed in the processor description.

9.4 Teleload ROM

The Teleload ROM contains a number of fixed program routines which are described in document 80012977. The ROM data is held at two separate bytes with different location addresses as detailed in TD sheets 5.7 and 5.8. When the most significant output from the four bit counter (described in section 9.3) is 0 the least significant byte of data is read out of the ROM and passed to the eight bit latch and hence to DIN lines 0-7. This data also appears on DIN lines 8 to 15 at this time. When the most significant output from the four bit counter is one the least significant byte of data is latched in the eight bit latch and the most significant byte of data read out from the ROM. This data is then placed on DIN lines 8 to 15 and the latch output placed on DIN lines 0-7 thus giving a full word of data.

Links can be set (TD sheet 4.6 reference D4) so that either the bottom four or bottom eight words of ROM replace the equivalent RAM store at addresses 0000 to 0003 (or 0007). This portion of the ROM contains a 'Bootstrap' routine. The third link position disables this portion of the logic so that the bottom portion of the RAM store may be used.

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10 DISPLAY COUPLER (2K Displays)

10.1 Introduction

The Display Coupler consisting of a Display Store and a Character Generator is contained on a single double height PCB (P003). Each coupler provides 2 x 2K displays each consisting of 25 lines of 80 characters. A block diagram of the coupler is in TD sheet 2.3 and a system operation diagram in TD sheet 6.14.

10.2 Displayed Character

The displayed character area is organised as 11 scan lines of seven dots per character (see figure 10.1).

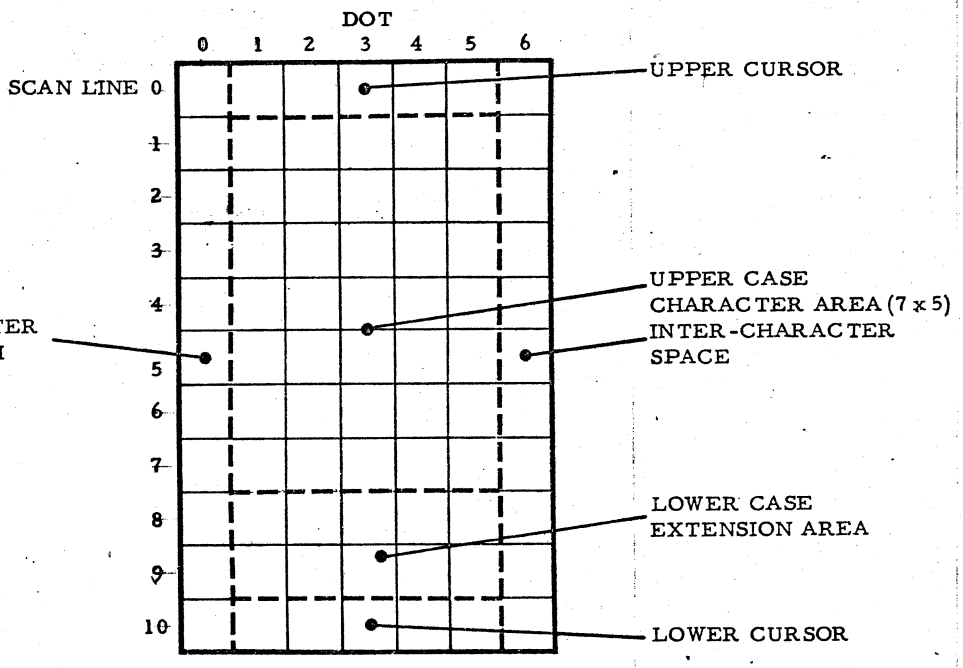

FIGURE 10.1 DISPLAYED CHARACTER AREA

The area from scan lines 1 to 9 inclusive (Dots 0-6) is specified by the character generator ROM (see section 10.11). The two cursor lines and the SOM (start of message) line are inserted by the hardware as required.

The characters are derived from a 1K x 8 bit ROM organised as 128 characters of eight rows each. Seven of the eight outputs are used for the five character dots and the two inter character spaces. The eight character specifies whether the character is upper or lower case, i.e. whether the character requires the lower case extension area.

The eight character rows from the ROM are displayed on scan lines 1 to 8 (line ADD0-7 see TD sheet 6.14) line 9 is character row 0 (i.e. a duplicate of scan line 1) and the shift bit selectively blanks lines 1 or 9 to give either lower or upper case characters.

All the available characters are detailed in TD section 7.

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10.3 Timing

All the timing is derived from the machine timing signals of TP1, TP2, TP3 and 10.752 MHz as detailed in section 10.9 and TD sheets 6.12 to 6.17.

The Dot Rate clock is derived directly from the 10.752 MHz highway line and is thus 10.752MHz (93ns) giving a character rate of 1.536 MHz (651ns).

Each scan line is timed to be 100 characters consisting of of 80 displayed characters and 20 characters flyback giving a scan line rate of 15.36 KHz (65μs). Each character row is made up of 11 scan lines which gives a character row rate of 1.396 KHz (0.72ms). Twenty six character rows comprise a screen of data giving a frame rate of 52.8Hz (18.9ms).

Frame flyback time has five additional scan lines (325μs) for frame synchronisation.

10.4 Display Store Addressing

The Display Store may either by addressed by the processor via the highway address lines or by the address generated in the Display Address Counter (see section 10.8).

The address from the processor is carried on ADDR lines 0-15. Lines 16 to 21 are not used by this store and any one of these lines going true will disable the store completely (see TD sheet 4.7 reference B1). The address lines 0-15 give a possible 64K word address range of which this store requires a 4K word address range. This is selected by means of links as detailed in TD sheet 4.7 and in the configurator 80014028. Address lines 0 to 11 are used to address the store chips within the 4K word range of addresses.

The highway Address line ADD 1 to 10 and the Display Address lines DISADD 1 to 10 are applied to a 2:1 multiplexor (TD sheet 4.7 reference B3). During the time when the scan lines 0 to 9 are being generated, the processor is allowed to access the store using the highway address lines therefore lines ADD 1 to 10 are allowed through the multiplexor (see TD sheet 6.14). During the intercharacter line the next row of characters is read out from the store therefore lines DISADD 1 to 10 are allowed through the multiplexor (see TD sheet 6.14).

The resulting output address from the multiplexor is split into the A and B address lines as detailed in TD sheet 6.15.

10.5 Hold

As the store does not operate at sufficient speed for the processor the highway HOLD line is used to slow down the processor when carrying out Display Store transfers (see TD sheets 6.2 and 6.3).

When Store Strobe isnot true the code 1011 (B) is loaded into the four bit down counter (TD sheet 4.7 reference H5). When Store Strobe goes true, provided NEXT is not true (see TD sheet 6.14) the bistable (TD sheet 4.7 reference G5) is reset, thus enabling the counter. At the same time provided the store is addressed by a valid address (i.e. provided SELECTED is true), Store Strobe true sets the D-type (TD sheet 4.7 reference G4) and thus gives HOLD. The counter now counts down on each positive going edge of the 10.752 MHz clock until a count of 0000 is reached when the CI output of the counter goes true thus resetting the D type and removing HOLD.

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If NEXT is true (see TD sheet 6.14) then the HOLD line is 'set' but the counter does not begin to count down until NEXT goes false. Thus the Store Strobe is extended to allow the next row of characters to be generated before the store transfer takes place.

10.6 Write Enable

When the Hold counter described in section 10.4 has counted down to 0111 (7) the Write line decoders are enabled, (TD sheet 4.7 references K5 and K6) thus allowing the highway address lines ADD0 and AD11 to Write enable the required store block.

10.7 Display Word

The Display Word consists of 12 bits allocated as detailed in figure 10.2.

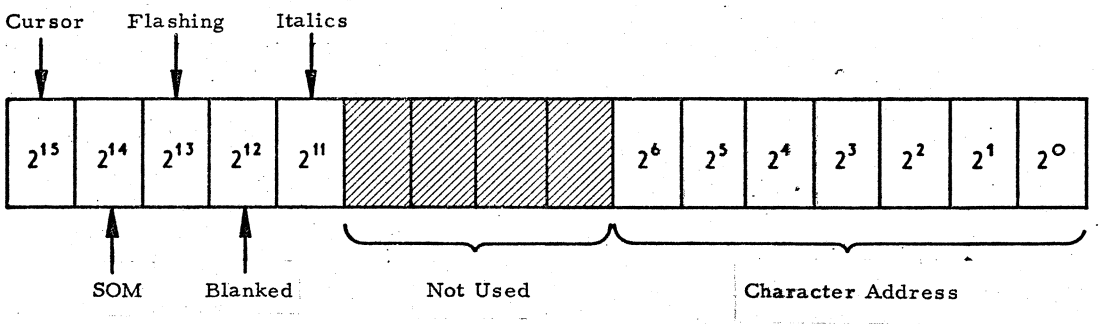

FIGURE 10.2 DISPLAY WORD

10.7.1 Cursor When set, the hardware inserts the cursor lines above and below the character (see section 10.14).

10.7.2 SOM When set, the hardware inserts a vertical dotted line 11 scan lines in height immediately before the specified character (see section 10.15).

10.7.3 Flashing When set the hardware flashes the character at 1.6Hz (see section 10.13).

10.7.4 Blanked When set, the character is blanked (see section 10.12).

10.7.5 Italics When set, the character is slanted at 14^{o} to the vertical with scan line 9 as the non shifted base. SOM and Cursor are also slanted (see section 10.18).

10.7.6 Blanked and Italics When both are set the seven bit character address is ignored and address $(00)_{10}$ applied to the Character Generator to specify a 'Start of Variable Field' character.

10.7.7 Character Address The seven bit character address applied to the Character Generator selects one of the 128 characters detailed in TD section 7.

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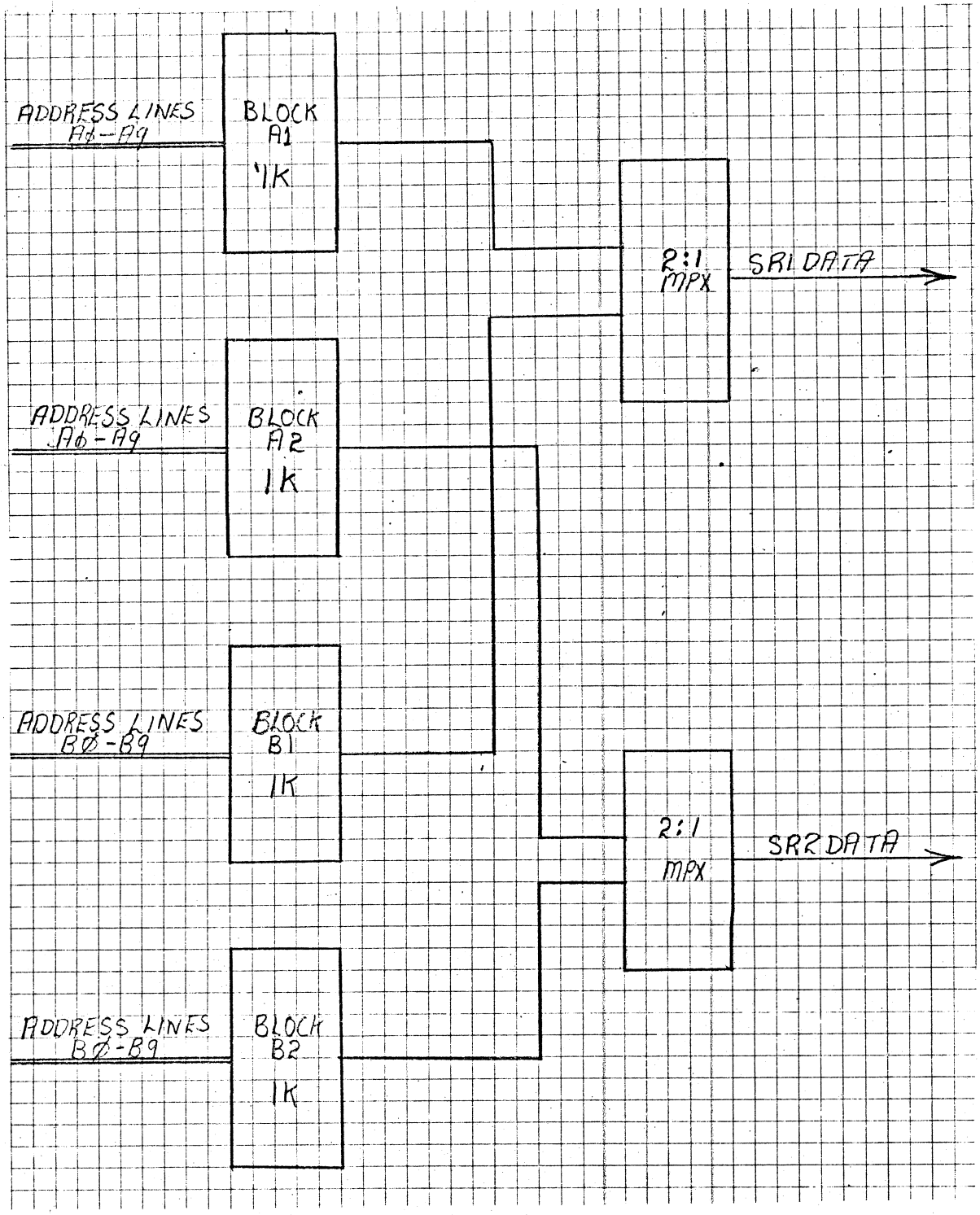

FIGURE 10.3 DISPLAY STORE ORGANISATION

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10.8 Display Store (see TD sheet 6.15)

The elements used to construct the 4K x 12 bit store have a cycle time approximately twice that required by the system therefore the store is organised as detailed in figure 10.3. For approximately 650ns the data words from store blocks A1 and A2 are routed through the two 2:1 multiplexors. For the next 650ns data is taken from store blocks B1 and B2 and routed through the multiplexors. The multiplexor then switches again to route data from store blocks A1 and A2. The outputs from the two multiplexors give the character addresses for the two display channels. All the store timing is detailed in TD sheet 6.15.

10.9 Display Address Counter

The display address counter bits 0-3 provides all the timing for the Display Coupler as detailed in TD sheets 6.12 to 6.15. This portion of the counter runs continuously.

Display address bits 4-10 are generated when NEXT and ENSR2 are true (see TD sheet 6.14) i.e. when the display is on line 9 of each character row.

10.10 Character Generator Addressing

The two data streams from the store system are loaded into the 80 bit shift registers SR1 and SR2 when NEXT is true i.e. when the display is on line 9 of each character row (see TD sheet 6.14).

When the data streams leave the store system they are in phase. As a common character generator is used it is necessary to arrange that the data streams are out of phase when they reach the character generator. This is achieved by first loading each word of the SR1 data stream into a parallel in/parallel out register (see TD sheet 4.8 reference B2). The output from this register is then loaded into the 80 bit shift register SR1 on the negative going edge of SRCLK. The SR2 stream is applied directly to the 80 bit shift register SR2 and is loaded on the positive going edge of SRCLK. The effect of this is to make SR1 and SR2 half an SRCLK cycle out of phase with SR2 leading (see TD sheet 6.16).

During the other 10 scan lines of each character row, i.e. NEXT false, the contents of the 80 bit shift registers are cyclic shifted thus giving two channels of character addresses plus information on hardware inserted characters (see section 10.7). The two shift register output channels are applied to a 2:1 multiplexor (see TD sheet 4.8 reference D2) which switches each channel in turn to the character generator (see TD sheet 6.17).

10.11 Character Generator (see TD sheet 6.17)

The output from the 2:1 multiplexor is still in the same form as was originally loaded into the display store therefore bits 0-6 form the character address and bits 11 to 15 determine if hardware inserted characters are required (see section 10.7).

Provided PROT (bit 11) and BLANK (bit 12) are not true together bit 0-6 (CHAR 0-6) are applied to the Character Generator ROM and provide address bits 3-9. Address bits 0-2 are provided by the Scan Line counter (TD sheet 4.8 reference A4). Provided the ROM is enabled (see sections 10.12 to 10.14) the complete address causes the ROM to output the dot pattern for each scan line of each character i.e. the 80 bit shift registers cycle once generating two channels of 80 addresses which are used to generate the first scan line of 80 characters for each channel. The registers then cycle again and outputs the same 80 addresses but as the scan line counter has advanced by one the second

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scan line of 80 characters is generated.

If both PROT and BLANK are both set CHAR 0-6 is inhibited and bits 3 to 9 of the ROM address are all zero. This address is the location of the 'Start of Variable Field Character' (see section 10.7.6).

10.12 Character Blank

If bit 12 of the display word is 'set' and provided PROT (bit 11) is not true the Character Generator ROM is disabled with the result the dot pattern for the addressed character is not generated.

10.13 Character Flash

The frame flyback timing pulse (FRAME F/B) see TD sheet 6.13 is applied to a four bit counter (TD sheet 4.8 reference D3) the outputs of which are applied to two D-types to give a final output which is true for 24 frame flyback pulses and false for eight pulses (i.e. 1.6 Hz).

When bit 13 of the display word is 'set' the 1.6Hz signal is used to alternately enable and disable the Character Generator ROM with the result that the character is displayed for 24 frames duration and then blanked for eight i.e. the character flashes.

10.14 Cursor

During scan lines 0 and 10 (addresses A and 9) (see TD sheet 6.14) the SYNC ROM sets CURSOR LINE true which disables the Character Generator ROM and enables the AND gate (TD sheet 4.8 reference F1).

If bit 15 (CURSOR) of the display word is set, then during scan lines 0 and 10 , the character dot pattern DOT 1-5 are forced true which causes the cursor lines on the display.

10.15 SOM

Bit 14 of the display word 'set' enables the AND gate (TD sheet 4.8 reference F1). Scan line address counter bit 0 (LINE 0) is applied to the same AND gate thus theoutput of the gate is true on alternate scan lines.

The output of the gate is wire ORed with the Character Generator ROM output DOT 0, thus DOT 0 is forced true every alternate scan line. This causes a vertical line of dots to appear on the display immediately before the addressed character.

10.16 Conversion of Parallel Dot Pattern to Serial Form (See TD sheet 6.17)

The parallel dot pattern from the Character Generator has to be converted to two streams of serial data before transmission to the two display units.

The generation of channel A is described here, channel B is identical except that the timing is different (see TD sheet 6.17).

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Assuming that initially A MODE is false DOT 6-0 is loaded into the least significant seven inputs of an eight bit shift register (see TD sheet 4.8 reference G2). The most significant input of the register is permanently connected to logic 1. The data loaded appears at the outputs of the register on the negative transition of SHIFT which is free running at 10.752 MHz. The most significant input has now caused A MODE to go true which in turn switches the register to shift mode. On the next negative transition of SHIFT the contents of the register are shifted down one place with the D input loaded into the top location (i.e. appears at A MODE). Thus provided the D input of the register is false the contents of the register will be shifted on each negative transition of SHIFT i.e. the parallel data is shifted out in serial form as DATA A.

When the D input goes true (i.e. LOAD A true and gate enabled) the contents of the register are shifted once more causing A MODE false which in turn switches the register back to the load mode. On the next negative transition of shift a new set of data is loaded into the register to start the cycle again.

During line flyback and frame flyback (LINE BLANK and FRAME F/B true) LOAD A is inhibited so no characters are output to the display at these times.

10.17 Character Shift

As described in section 10.2 scan lines 1 and 9 Addresses 0 and 8 are selectively blanked to provide either upper or lower case characters.

If the shift output from the Character Generator ROM (SHIFT BIT) is set, then during scan line address 8 (i.e. A LINE 8 true) LOAD A is inhibited thus blanking that line of the character giving an upper case character. If SHIFT BIT is not set then during scan line address 0 (i.e. A LINE 0 true) LOAD A is inhibited, thus blanking that line of the character and giving a lower case character.

10.18 Slanted Characters

When bit 11 (PROT) of the display word is 'set' the displayed character is slanted, provided the 'Protect' link is 'set'. Channel A is described here, channel B operates in the same way.

The state of bit 11 is staticised in the D-type (TD sheet 4.8 reference H2) as A MODE goes true, i.e. at the beginning of the character line. (See section 10.16.)

If PROT is true then when staticised this disables UPRT DATA and enables SLANT DATA. The serial data (DATA A) is then applied to a 300ns delay line which is tapped at 37.5ns intervals. An 8:1 multiplexor (TD sheet 4.8 reference K2) is used to pick off the required delay for each scan line.

During scan lines 9 and 10 (address 8 and 9) MIN SLANT is true which disables SLANT DATA so no delay is applied to these scan lines.

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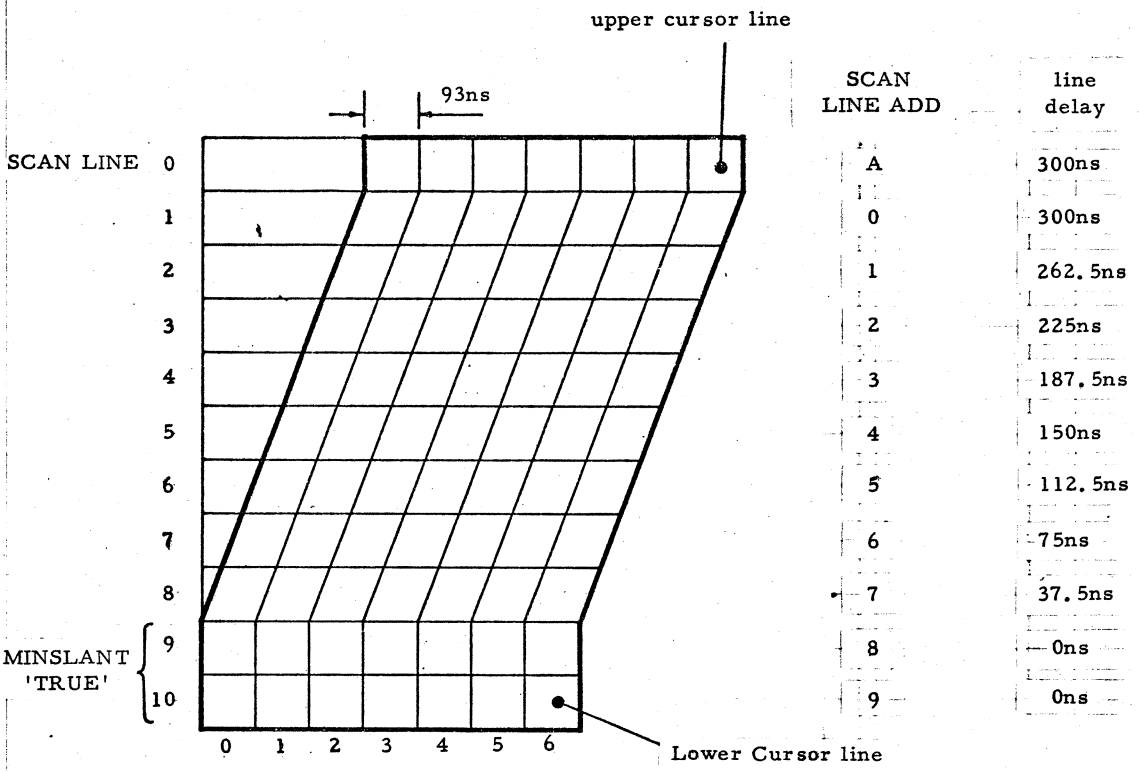

FIGURE 10.4 SLANTED CHARACTERS

10.19 Upright Characters (Channel A described; channel B identical)

When bit 11 of the display word is not set UPRT DATA is enabled and SLANT DATA is disabled (see section 10.18). DATA A is applied to the enable of the 8:1 multiplexor (TD sheet 4.8 reference K2.) When DATA A is true the output of the multiplexor is forced high which then causes a 'dot' on the display. When DATA A is false the addressed output from the delay line is allowed through to the multiplexor output.

When the preceding character is slanted then the display for the area shaded in figure 10.5 will be an OR of the two characters as the delay line will still contain data from the previous character.

When the preceding character is upright then the delay line will contain all zeros. Therefore when the multiplexor is enabled by DATA A false, the output of the multiplexor is false causing a blank on the display.

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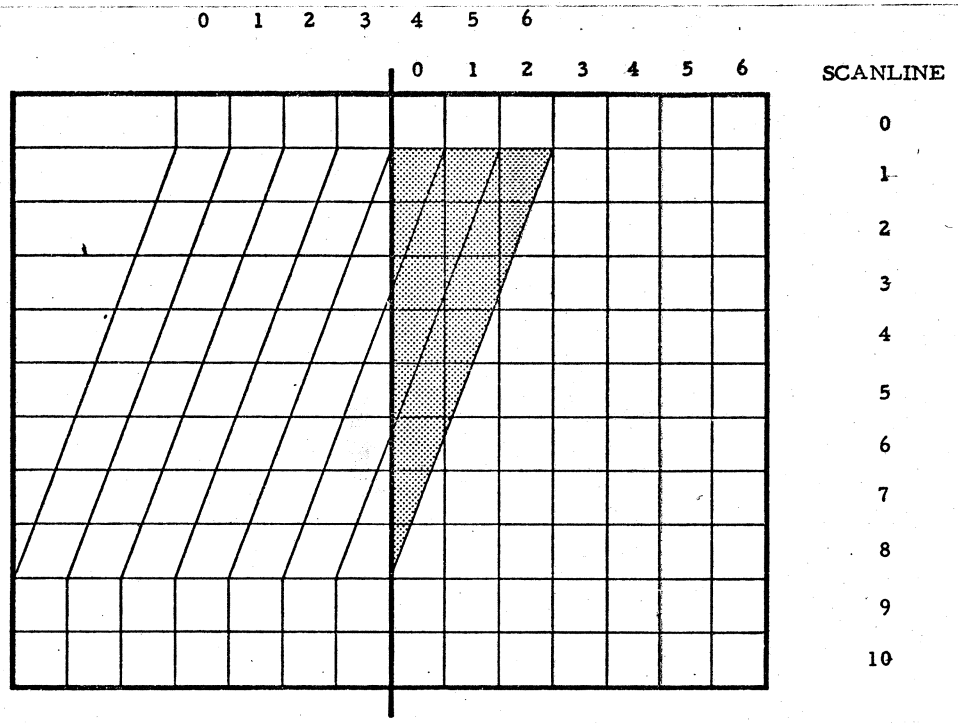

FIGURE 10.5
CHARACTER DISPLAY WHEN SLANTED CHARACTER IS FOLLOWED BY AN UPRIGHT CHARACTER

10.20 Composite Video Output

The Video Display Data and the Composite Sync Pulse are applied to a 'special' line driver element to give a composite Video Output as detailed in figure 10.6.

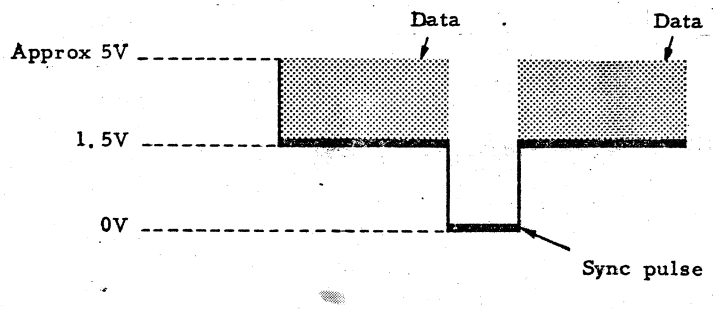

FIGURE 10.6 COMPOSITE VIDEO OUTPUT

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Sheet 10.10

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11 DISPLAY COUPLER (1K Displays)

To be issued

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Number 80011824
Sheet 11-2

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12 INPUT/OUTPUT COUPLER

12.1 Introduction

The Input/Output Coupler is contained on a single PCB (P004) and provides an interface between the Terminal Controller Highway (see section 5) and the devices defined in table 12.1.

Note: Other devices with a similar interface may be connected.

Device	Quantity	Comments
Modem	1	Coupler capable of full duplex operation
Termiprinters or Teletypes	2	Coupler capable of full duplex operation
Keyboards	4	Of a type as described in 80011126

TABLE 12.1 INTERFACED DEVICES

The coupler also carries a Parameter Table containing 36 bytes of information referring to the type, quantity and use of each device connected to the coupler.

12.2 Device Addressing

The Device Address range is selected by means of links (TD sheet 4.9 reference B1) and is derived from the DEV ADD lines 3, 4 and 5 (see table 12.2). Within each address range the Device Addresses (carried on DEV ADD lines 0-2) are fixed as detailed in table 12.3 where X is the address range selected.

Link Position	Pins Linked	DEV ADD			Address Range Selected	
		5	4	3	HEX	OCTAL
1*	1-16	0	0	0	00 - 07	00 - 07
2	2-15	0	0	1	08 - 0F	10 - 17
3	3-14	0	1	0	10 - 17	20 - 27
4	4-13	0	1	1	18 - 1F	30 - 37
5	5-12	1	0	0	20 - 27	40 - 47
6	6-11	1	0	1	28 - 2F	50 - 57
7	7-10	1	1	0	30 - 37	60 - 67
8	8-9	1	1	1	38 - 3F	70 - 77

* As Device Address $(00)_{16}$ corresponds to the Watchdog Timer (see section 6.14), link position 1 must not be used.

TABLE 12.2 ADDRESS LINKS

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Address	Device
$(X0)_8$	Modem Buffer
$(X2)_8$	Parameter Table
$(X3)_8$	Keyboard Buffer
$(X4)_8$	Printer 1 Buffer
$(X5)_8$	Printer 2 Buffer

Notes: 1 X is selected address range (see table 12.2)

2 Device Addresses $(X1)_8$, $(X6)_8$ and $(X7)_8$ are not recognised by the I/O Coupler and are therefore available for used by other types of coupler.

TABLE 12.3 DEVICE ADDRESSES

12.3 Transfer Acceptable

A valid address with Device Strobe (DEVSTR) true gives Transfer Acceptable (TRAN ACC) true (see TD sheet 4.9 reference C1).

12.4 Command Decode (see TD sheet 4.9)

The basic Device Commands are carried on Store Address lines 6 and 7 (SADDR 6, 7) and provided Device Strobe is true are decoded as detailed in table 12.4.

Store Address Lines		Command
7	6	
0	0	Read Data
0	1	Write Data
1	0	Read Control (Status)
1	1	Write Control

TABLE 12.4 COMMAND DECODE

12.5 Write Control Word

The bits defined in table 12.5 are standardized; the remainder are defined for each individual buffer.

DOUT	Control Function
2^0	Terminate Device: Cancels any existing service requests on addressed 'buffer' and prevents further service requests until a defined start condition has occurred
2^6	Write Channel Addressed
2^7	Read Channel Addressed *

* Indicates to a buffer supporting full duplex transfers which direction is to respond to the Write Control Command (see also table 12.6)

TABLE 12.5 STANDARD WRITE CONTROL BITS

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12.6 Device Commands (see TD sheet 4.9 D 3/4)

The basic commands (see table 12.4) are combined with the standardized Write Control bits to give the Device Commands defined in table 12.6. The three least significant bits of the device address are used to route the command to the correct device buffer.

Basic Command	DOUT			Device Command
	2^7	2^6	2^0	
Read Control	-	-	-	Read Control
Write Data	-	-	-	Write Data
Write Control	-	-	-	Write Control
Read Data	-	-	-	Read Data *
Write Control	1	0	1	Read Terminate *
Write Control	0	1	1	Write Terminate

* Read Data and Read Terminate appear on the same control lines

TABLE 12.6 DEVICE COMMANDS

12.7 Service Requests

All the various device buffer Service Request lines are combined onto the highway Service Request line by a multiplexor (TD sheet 4.9 reference F5), which is controlled by the least three significant bits of the device address. Therefore, when a device recognises its own address and has a Service Request outstanding it raises the highway Service Request line (see section 6.11).

12.7.1 Parameter Table Service Requests The Parameter Table cannot raise a Service Request.

12.7.2 Modem Buffer Service Request A Modem Buffer strapped for receipt of asynchronous data raises a Read Service Request (MI RD REQ SER) on receipt of a character preceded by a valid start bit.

A Modem Buffer strapped for receipt of synchronous data raises a Read Service Request upon reception of a character following initial detection and deletion of ISO SYN character $(16)_{16}$.

The software will respond to the Read Service Request by issuing a Read Data Command (or Read Terminate Command). Each subsequent byte of data, when received, will give rise to a Modem Read Buffer Full signal (see section 12.15), which in turn generates a Read Service Request. The software will respond to these subsequent Service Requests with either a Read Data or Read Terminate Command (see section 12.6). The Read Data Command must be issued within one character time of detection of the Buffer Full condition to ensure no loss or corruption of data.

A Write Service Request is raised following the issue of a Write Data Command. The Service Request will not be raised until the modem returns the signal 'Ready for Sending' (RFS) and therefore indicates to the software that the Transmit Modem Buffer is empty and the modem is ready to transmit data.

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During synchronous transmissions the transmit Buffer Empty condition is masked for two bit times per character (this is to overcome logic constraints in the LSI chip). As a result the Service Request following the initial Write Data Command may be raised and then removed before it is honoured. The pre-Service Request Conditions may remain true for a maximum of n-2 bit times (n is the number of bits in a byte) but for a minimum of less than one bit time.

The software will respond to a Write Service Request with either a Write Data or Write Terminate Command. To ensure a continuous flow of uncorrupted data from a Transmit Modem Buffer which is strapped for synchronous transmission, a Write Data command must be issued within n-2 bit times (n is the number of bits in a byte) of detection of the buffer empty condition.

12.7.3 Printer Buffers Service Requests are raised in a similar way to Service Requests for asynchronous Modem Buffers.

The software will respond to a Write Service Request with either a Write Data or Write Terminate Command.

A Read Service Request will cause the software to issue either a Read Data or Read Terminate Command. To ensure that there is no loss or corruption of data a Read Data Command must be issued within one data time of the detection of the buffer full condition.

12.7.4 Keyboard Buffer Service Requests The Keyboard Buffer raises a Service Request when the buffer detects that a keyboard key (or Badge or Key Reader bit) has changed state from that previously recorded.

The conditions pertaining at the time of the Service Request will remain true until the software replies with either a Read Data or Read Terminate Command. Data placed on the highway DIN lines 8-15 during a Read Terminate Command is ignored by the Processor. Therefore the software record of the state of a keyboard may not match the actual state following a Read Terminate Command.

12.8 Data Output (to Highway)

The data from the Modem and Printer Buffers to the highway is routed to the highway via a 2:1 multiplexor (TD sheet 4.10 reference D2/3) when Device Strobe is true.

12.9 Hold (see TD sheet 6.7)

The Hold facility is used to stop the processor and thus extend Device Strobe for approximately 2.5μs during data and command transfers. This ensures that data is stable on the highway DIN lines when the processor accepts it following the release of HOLD. During command transfers the Hold facility ensures the coupler has had sufficient time to decode the commands correctly.

12.10 Clock Configurations

The clocks are selected to suit the Modem and printers connected to the coupler and the desired transmission and reception rates. The links are defined in the configurator 80014028 and section 12.10.2 of this document.

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12.10.1 Modem Buffer Clocks The Modem Buffer can be configured to operate with either of the two most common modems e.g. Modem 1 or Modem 7. The third alternative of direct connection to the main frame is also possible. The switch settings for the clocks for these three methods of operation are defined on the configurator 80014028.

12.10.2 Printer Buffers Clocks The four channels (two transmit and two receive) can operate at different data transfer rates selected by means of links. Table 12.10 details the speeds and the DIL pin to be selected for that speed, table 12.8 details the DIL pin for each printer channel. Therefore to select a desired speed for a particular channel the speed pin should be linked to the appropriate channel DIL pin.

Clock Rate (Hz)	Data Rate (Baud)	DIL 10E Pin No
16x9600	960	16
16x4800	480	15
16x2400	240	14
16x1200	120	13
16x 600	60	12
16x 300	30	11
16x 200	20	10
16x 110	11	9

TABLE 12.7 PRINTER CHANNELS DATA RATE SELECTION

Printer Channel	DIL 10E Pin No
P1 Tx	1
P1 Rx	2
P2 Tx	7
P2 Rx	8

TABLE 12.8 PRINTER CHANNELS CLOCK LOCATION

12.10.3 Modem Clock (DIL09E pin 12) This is a test signal used when conducting back to back tests.

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12.11 Parameter Table

The Parameter Table is a block of Read Only Memory comprising a set of switches and a ROM chip. It is used to define to the system some or all of the following:

(a) Link Level Address

(b) Number of Visual Display Units and Keyboards

(c) Number of Printers

(d) Printer to Video patching

(e) Which Main Frame the Terminal Controller is connected to (i.e. 1900, System 4) etc

The Parameter Table has 'port' address $(X2)_8$ (see section 12.2) and within this address the highway Store Address lines 8-13 are used to address 36 'sub-ports' each containing a single byte of information related to the above list.

A description of the organisation and configuring of the parameter table is not included here but may be found in the software documentation and configurator 80014028 respectively. The coding for the ROM is in TD sheet 5.10.

12.12 Modem Buffer (see TD sheet 4.11)

The Modem Buffer is designed round two LSI elements, one a Terminal Receiver and one a Terminal Transmitter. The Buffer can be configured to operate in either synchronous or asynchronous mode (see section 12.10 for clock configuration).

12.13 SYN Character Detection

The first character in a received synchronous message is always an ISO SYN character $(16)_{16}$ which is detected to achieve character synchronisation.

Before SYN is detected SYN DETD is false (TD sheet 4.10 reference C1). Provided the receiver is strapped for synchronous data i.e. MIRx ASYNC false and that DEV STRBE is false, (i.e. the Buffer is not busy) then the 2:1 multiplexor (TD sheet 4.10 reference D2/3) will be enabled to pass received modem data.

A SYN character arriving with the above conditions true is detected by the SYN character detector (TD sheet 4.10 reference E2) to give MISAMPLE SYN RECOG true. At a time determined by the internal I/O coupler status scanner (see TD sheet 6.18) MISAMPLE SYN RECOG sets the bistable (TD sheet 4.11 reference C4) and sets SYN DETD true which then inhibits further SYN detection.

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12.14 Modem Buffer Receive Channel (see TD sheet 4.11)

12.14.1 Synchronous Mode In this mode data is received in a continuous serial form with no 'start' or 'stop' bits. It is therefore necessary to obtain both bit and character synchronisation in order to receive a valid message. Bit synchronization is achieved in the LSI chips so is not described in this document.

With SYN DETD false (see section 12.13) the buffer storage shift register in the LSI chip is 'transparent' therefore received data can be monitored as it ripples through the register.

The first character in a message is always an ISO SYN character $(16)_{16}$ which is detected as described in section 12.13. When SYN is detected giving SYN DETD true the buffer storage shift register in the LSI chip switches to normal mode.

The second character in the message which should also be an ISO SYN character $(16)_{16}$, is then stored in the LSI chip and causes a 'Buffer Full' output from the LSI chip. Buffer Full causes a Read Service Request which the software answers with a Read Command. The software then verifies the second SYN character and further received characters are processed as data.

The software terminates the data stream with a Read Terminate command which resets the SYN DETD bistable and switches the buffer storage shift register back to 'transparent mode'.

12.14.2 Asynchronous Mode The Modem Rx Buffer is configured for Asynchronous Data by setting the clock as detailed in section 12.10 and by connecting M1RxASYNC 'high'.

A character of asynchronous data is always preceded by a 'Start' bit and always followed by at least one 'Stop' bit. When the receiver detects a 'Stop' bit logic in the LSI chip synchronizes the LSI internal clock with the mid point of the 'Start' bit. If the Start bit disappears during this synchronization period the receiver reverts back to looking for a 'Start' bit.

Once the 'Start' bit has been detected and synchronization obtained the LSI chip reads in the rest of the character and the 'Stop' bit. Once the complete character has been read in the LSI chip raises a 'Buffer Full' signal which causes a Read Service Request. The software replies to this service request with either a Read Data or Read Terminate Command which causes the data to be read out onto the highway and resets the LSI chip to looking for a 'Start' bit.

Absence of a Stop bit at the end of a character sets the status bit 2^0 (BRK), (see section 2.18).

12.15 Modem Buffer Transmit Channel

12.15.1 Synchronous Mode When no Write Data command has been issued to the Modem Buffer (i.e. idling state) a series of all ones $(FF)_{16}$ are assumed and processed by the LSI Transmitter chip. A bit count per character is therefore continually cycling. A M1WRDATA command causes data on DOUT lines 2^0-2^7 to be loaded into the LSI Transmitter chip. This data is then transferred in the LSI chip to a shift register at n-1 bit time (where n is the number of bits in a byte). At n-2 bit time SYN TRANSFER is true and remains so for two bit times. This in turn causes BUFF EMPTY true which inhibits the raising of a Service Request during this time. After this time a Service Request

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is raised.

The data in the LSI shift register is shifted out to the CCIT transmitter in serial form at a rate determined by DIVIDED Tx CLOCKM1 (see section 12.10). As the last two bits of the data word are shifted out SYN TRANSFER goes true so the Write Service Request is removed. It therefore follows that to ensure a continuous flow of data the software must reply to the service request with a new Write Data Command within n-2 bit times of the service request being raised (n is the number of bits in a word).

A message is terminated by a Write Terminate Command.

12.15.2 Asynchronous Mode The Modem Buffer is configured for asynchronous data by setting the clock as detailed in section 12.10 and by connecting M1Tx ASYNC 'high'. This causes the LSI chip to generate 'Start' and 'Stop' bits which are inserted in the data flow at the output at appropriate places.

Either one or two 'Stop' bits can be inserted. The LSI input M1Tx 2 STPBIT true causes two 'Stop' bits to be inserted, the input false causes one 'Stop' bit to be inserted.

Transmission of a message is started by a Write Data Command (M1WRDATA) which loads the first character of the message into the input buffer of the LSI chip. This causes the LSI chip to generate the output, BUFFER EMPTY false.

At the same time M1WRDATA is statisised in the bistable TD sheet 4.11 reference G5 and thus raises the modem signal RTS (Ready to Send).

The system now waits for the modem to return the signal RFS (Ready for Sending). When this signal is returned, this together with the BUFFER EMPTY false condition causes SYSTEM READY true. (SYN TRANSFER always false during asynchronous operation).

The data word held in the LSI input buffer is now transferred to the LSI output shift register and BUFFER EMPTY goes true. This in turn raises a Write Service Request and removes the SYSTEM READY input. The data is now shifted out to the CC1TT transmitter in serial form at a rate determined by DIVIDED Tx CLOCK M1 (see section 12.10).

The software will reply to the service request with a Write Data Command which again causes data to be loaded into the LSI input buffer. This again causes BUFFER EMPTY false but as RTS and thus RFS have not been removed SYSTEM READY true is thus immediately generated. The second word of data is therefore transferred to the LSI output register with the result BUFFER EMPTY goes true and raises a Write Service Request. At this point the second word of data is shifted out to the CCITT transmitter.

Data will continue to be transferred in this form until the message is terminated by a Write Terminate Command (M1WRTERM). This command resets the M1WRDATA bistable which in turn inhibits further service requests and removes the modem signal RTS. The Modem Transmit Buffer therefore reverts to the state as existed before the beginning of the message transmission.

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12.16 Modem Buffer Word Length

Both the transmitted and received word lengths can be selected by means of the word length selection inputs on the LSI chips. Table 12.9 details the word length selection.

M1 Tx WORD LENGTH SELX M1 Rx WORD LENGTH SELX	M1 Tx WORD LENGTH SELY M1 Rx WORD LENGTH SELY	Word Length
0	0	5 bits
1	0	6 bits
0	1	7 bits
1	1	8 bits

TABLE 12.9 MODEM BUFFER WORD LENGTH

12.17 Modem Buffer Write Control Word

In addition to the standard Write Control bits defined in section 12.5 bit 2^2 is used to 'set' the modem line CDSL (Connect Data Set to Line)

12.18 Modem Buffer Status Word

A Read Control Command to the Modem Buffer causes the buffer status to be reported on the highway DIN lines. The Status Word is defined in table 12.10.

Bit	Set to	Meaning
2^0	1	Rd Break (ASYNC operation only: see section 12.14.2)
2^1	1	Overrun (Read Service Request not answered in time)
2^2	0	DSR
2^3	0	RLS
2^4	0	RFS
2^5	1	Parity Error (see Note 1 below)
2^6	1	Write Service Required (see Note 2 below)

Notes: 1 The Modem Receive Buffer LSI chip is permanently connected to check for 'odd' parity.

2 The Status bit 2^6 is set if either a Write Service is required or if the modem line CLI (Calling Line Indicator) is set.

TABLE 12.10 MODEM BUFFER STATUS WORD

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12.19 CCITT Interface

All Modem Buffer/Modem connections are at CCITT levels. The connections are detailed in table 12.11.

Signal	Meaning	Comments
RSET	Modem Rx Clock	
TSET	Modem Tx Clock	
RLS	Received Line Sending	Data Carrier Detect
DSR	Data Set Ready	
RTS	Request To Send	Used on Async
RFS	Ready For Sending	Transmission
RxD	Received Data	
TxD	Transmitted Data	
CDSL	Connect Data set to line	
CLI	Calling Line Indication	

TABLE 12.11 CCITT INTERFACE

12.20 Printer Buffers

The two identical Printer Buffers are based around two LSI UART's (Universal Asynchronous Receiver/Transmitter). The buffers operate in full duplex mode. The word length parity and number of 'stop' bits can be selected by means of links (see sections 12.23, 12.24 and 12.25).

12.21 Printer Buffers Receive Channels

A character of asynchronous data is always preceded by a 'Start' bit and always followed by a 'Stop' bit. The UART receiver detects a 'Start' bit by looking for a mark to space transition and then sampling the input during the following eight clock periods. (Clock is P Rx CLOCK and is set as detailed in section 12.10 2.)If the input line returns to mark (i.e. because of noise during any of the eight clock periods the UART receiver reverts to idle and looks for another 'Start' bit.

If a valid 'Start' bit is received the data word is shifted into the UART receiver on each succeeding 16th clock period after the eight clock period 'Start' bit validation. Once the complete data word has been shifted into the UART receiver it is checked by internal logic (in the UART) for parity and framing errors and the result placed in an internal status holding register.

As the UART receiver samples the first 'Stop' bit it also checks the data output register to check if previous data has been read out and if not sets an overrun signal in the status holding register. One clock period later the data and status bits are shifted in parallel to the UART data output register and the UART output signal DA (Data Available) is set.

At a time determined by the internal I/O coupler status scanner (see TD sheet 6.18) P1 (or 2)SS is set which strobes the UART status register and places the status bits on the output lines. At the same time the trailing edge of P1 (or 2)SS strobes the Printer Service Request bistable and latches the state of the UART DA output. Therefore if DA is set indicating data available a Printer Read Service Request is raised i.e. P1 (or 2) RDREQSER.

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The software will reply to a read service request with either a Read Data or Read Terminate Command which strobes the data word out from the UART and onto the highway. At the same time these commands reset the service request bistable and the status register and DA output in the UART.

12.22 Printer Buffers Transmit Channels

The data word to be transmitted is applied to the data inputs of the UART in parallel form and is temporarily stored in a holding register as a Write Data Command. The UART then checks the status of its transmitter to determine if a previous character has been transmitted. If so the data is transferred along with the start, parity and stop bits to an internal serial shift register. The data is then shifted out from the serial register and transmitted in a serial form with the 'Start' bit first on each 16th clock period (P1 (2) Tx CLOCK is the clock rate and is set as detailed in section 12.10.2).

As the data is transferred from the temporary input holding register to the serial shift register the UART output TBMT is set to indicate that the input buffer is empty.

At a time determined by the I/O coupler internal status scanner P1 (or 2)SS is set, which latches the state of the UART TBMT output into the Write Service Request bistable. Therefore if TBMT is set indicating the UART input holding register is empty a Write Service Request is raised. The software will reply to this Service Request with either another Write Data Command to load further data into the UART or a Write Terminate Command which resets the Write Service Request bistable.

It therefore follows that if a character is loaded during the transmission of the previous character the 'Start' bit for the new character will immediately follow the last 'Stop' bit of the previous character.

12.23 Printer Buffers: Transmitted Stop Bits

The number of 'Stop' bits inserted in a character by the UART transmitter can be selected by means of a link. P1 (2) 2 STP BIT linked to 0V causes one 'Stop' bit to be transmitted and conversely when linked to +5V two 'Stop' bits are transmitted.

12.24 Printer Buffers: Word Lengths

The word length for each printer channel can be selected by means of the word length selection inputs on the UART's. Table 12:12 details the word length selection.

P1 WORD LENGTH SELY P2 WORD LENGTH SELY	P1 WORD LENGTH SELX P2 WORD LENGTH SELX	Word Length
0	0	5 bits
0	1	7 bits
1	0	6 bits
1	1	8 bits

TABLE 12.12 PRINTER BUFFER WORD LENGTH

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12.25 Printer Buffers Parity Select

If P1 (2) NOPARITY is set high the parity bit is removed from transmitted data and the receiver parity check is disabled.

P1 (2) EVEN PARITY set high sets the printer channel for even parity. When the signal is set low the channel is set for odd parity.

12.26 Printer Buffers: Write Control Word

The standard Write Control bits as defined in section 12.5 are the only ones used by the Printer Buffers.

12.27 Printer Buffers: Status Word

A Read Control Command to a Printer Buffer causes the Buffer Status to be reported on the highway DIN lines. The Status Word is defined in table 12.13.

Bit	Set to	Meaning
2^0	1	Rd Break (Frame Error)
2^1	1	Overrun (Read Service Request not answered in time)
2^2	0	DSR
2^3	0	RLS (Motor off)
2^4	1	Paper Low
2^5	1	Parity Error
2^6	1	Write Service Required

TABLE 12.13 PRINTER BUFFERS STATUS WORD

12.28 Keyboard Buffer (Normal Operation)

The buffer is controlled by a sequencing microprogram (see TD sheet 5.10). When the Keyboard Buffer is operating normally i.e. with no commands present as when following a GEN RES, each keyboard key in turn is interrogated to determine if that key has changed state since it was last interrogated. If the key has changed state a Service Request is raised and the Keyboard Buffer microprogram is frozen until the software answers the Service Request.

The microprogram address is generated by a free running (unless a K/B Service Request exists) four bit up counter (see TD sheet 4.13 reference E4).

Assume the microprogram starts at address 00, then when the microprogram reaches address 02 SWITCH is set which then increments the Time Slot Counter (TD sheet 4.13 reference D1). The Time Slot Counter is an eight bit up counter which generates a key (or key reader bit) address for each cycle of the microprogram. KBWRACT is false so the time slot counter output is routed through the 2:1 multiplexor (TD sheet 4.13 reference F2) to SEL 2^8 to 2^{15}.

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During the next eight microsteps 04 to 0A GATE SEL is set which enables the 8:1 multiplexor (TD sheet 4.13 reference G2). The most significant three bits of the microstep address are applied to the address lines of the multiplexor thus during the eight microsteps each of the SEL lines 2^{15} to 2^{8} are switched to the multiplexor output and so give a serial data stream.

The output from the 8:1 multiplexor is applied to the 2^{1} address line of the Forward Bit Encoding ROM. All other address lines are false therefore the ROM switches between location addresses 00 and 02 which are coded $(0F)_{16}$ and $(00)_{16}$. Therefore each of the SEL bits gives rise at the output of the ROM to four parallel bits of identical data.

The ROM output is buffered in a four bit parallel register (TD sheet 4.13 reference J3) and is then applied to the four keyboard transmitters.

It can therefore be seen from the above description that all four keyboards are interrogated at the same time. Microsteps 0B-11 allow time for the keyboards to be interrogated and for data to be returned to the keyboard buffer.

At microstep 12 RES Rx is true which resets the Received Data bistables (TD sheet 4.13 reference F5). During microsteps 13 to 15 GATE K/B RxD is true which enables the strobe (DBLEK/BCLK) to the Received Data bistables. The R-C network on the data inputs of the Received Data bistables gives noise protection. A pulse of received data causes the appropriate R-C network to ramp up the data input to the appropriate Received Data bistable and when the ramp reaches logic 1 level (approximately 650ns) the data is latched into the bistable. If the data pulse disappears before 650ns (noise) the data input immediately returns to logic 0 level.

During microstep 16 STORE READ is true. The output from keyboard seven Received Data bistable (RxK/B7) is routed through the 4:1 multiplexor (TD sheet 4.13 reference G6) and compared with the data stored in the 1K RAM store (TD sheet 4.13 reference H6) the previous time that the addressed key on keyboard four was interrogated. If the data differs i.e. the key has changed state then a Keyboard Service Request (K/B REQSER) is raised. During the next microstep (microstep 17) STORE WRITE is true and the data from the keyboard seven key is stored in the 1K RAM store if the data changed. The same cycle occurs for keyboards five, six and four during the next six microsteps although only the first keyboard to indicate a key changing state will raise the Service Request.

During microstep 1E INHμPROG is true which freezes the microprogram counter if a Service Request is outstanding. The microprogram remains frozen until the software has cleared the Service Request.

The software will issue a Sense Status Command to determine the cause of the Service Request (i.e. whether from a previous command see sections 12.29 to 12.32). The software will then issue a Read Data Command (K/BRD) (but see section 12.30). This command causes SEL 2^{8} - 2^{15} to be placed on the highway DIN lines 8-15 so identifying the 'time slot' i.e. the key. It also causes the contents of the 'Received Data bistables' (RxK/B4-7) to be placed on highway DIN lines 4-7. The software then processes this data to determine which keys on which keyboards have changed state. K/BRD true resets the Service Request bistable (TD sheet 4.13 reference K6) which removes the Service Request and allows the microprogram to advance and thus return to microstep address 00.

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12.29 Keyboard Buffer Write Control Word

In addition to the standard Write Control bits defined in section 12.5 the bits defined in table 12.14 are used. These bits are used to initiate various functions of the Keyboard Buffer which are described in sections 12.30 to 12.32.

DOUT Bit	Set to		Described in Section
2^3	1	Rescan Time Slot	12.30
2^4	1	256 Scan (0 = 128 Scan)	12.31
2^5	1	Report all Keystates	12.32
2^8	X	Rescan Time Slot address (2^3 set)	12.30
2^9	X		
2^{10}	X		
2^{11}	X		
2^{11}	X		
2^{12}	X		
2^{13}	X		
2^{14}	X		
2^{15}	X		

TABLE 12.14 KEYBOARD BUFFER WRITE CONTROL BITS

12.30 Rescan Time Slot

In this mode the Keyboard Buffer interrogates a particular key specified by the data on DOUT lines 8-15. This Write Control Command is normally issued following a Service Request but preceding a Read Data Command.

K/B WRCTRL and DOUT 2^3 'set' sets the Rescan Time Slot bistable (TD sheet 4.13 reference B2) giving RESCANTSX true and latches the data on DOUT lines 8-15 into the eight bit latch (TD sheet 4.13 reference D2). The Write Register bistable (TD sheet 4.13 reference B1) is also set by the above above conditions giving K/B WRB true.

When the microprogram reaches step 02 and sets SWITCH the strobe to the Time Slot Counter and the Write Active bistable is enabled. Therefore K/B WRB true is latched into the Write Active bistable to give K/B WRACT true. This condition disables the Time Slot Counter therefore a new time slot is not generated. K/B WRACT true also switches the 2:1 multiplexor (TD sheet 4.13 reference F2) so that the output from the eight bit latch is routed to the SEL lines.

The microprogram advances as described in section 12.28 until it reaches step 16 where data is compared. At this point as RESCANTSX is set a Service Request is automatically raised which is answered as detailed in section 12.28. Rescan Time Slot can thus be used to examine to state of any key out of sequence.

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12.31 256/128 Time Slot Scan

The Keyboard Buffer can be set to generate either 128 or 256 time slots. When set for 128 time slots the buffer only scans the keyboard keys (this is the normal state following a GEN RES). When set for 256 time slots, any key reader or badge reader bits are scanned also.

A K/B WRCTRL with DOUT 2^4 true sets the 128/256 scan bistable (TD sheet 4.13 reference D1) which enables the 2^{15} output from the Time Slot Counter thus setting the buffer to generate 256 time slots.

The buffer can only be reset to generate 128 time slots by a second K/B WRCTL with DOUT 2^4 not true.

12.32 Report All Keystates

In this mode the Keyboard Buffer reports to the software the actual state of each key scanned.

A K/B WRCTRL with DOUT 2^5 true 'sets' the Report Actual bistable and 'sets' REPACT (see TD sheet 4.13 reference B3). The microprogram cycles normally generating time slots but when step 16 is reached a Service Request is always raised which the software answers as detailed in section 12.28. In this way the software examines the data returned from every key or keyreader bit interrogated.

This mode can only be reset by a second K/B WR CTRL with DOUT 2^5 false.

12.33 Keyboard Buffer Write Command

A Write Command is used to change the state of the lamps and buzzer on each keyboard.

A Write Command (K/B WR DATA true) sets up the same conditions as for Rescan Time Slot (see section 12.30) and latches the data on DOUT lines 8-15 plus 2^4 to 2^7 into the eight and four bit latch respectively. The microprogram advances normally using the data from DOUT lines 8-15 as the SEL lines until step 0B when GATE FWD is true. At this point the data from the four bit latch is used to address the Forward Bit Insert ROM and cause a forward data bit to be generated following bit 2^8 of the time slot addresses (see TD sheet 5.11 for ROM coding).

The microprogram again advances normally but any received data is ignored and no Service Request raised.

The lamps are identified by DOUT lines 8-11 as detailed in table 12.15.

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DOUT 11	10	9	8	Lamp	Action
0	0	0	0	1	resets lamp
0	0	0	1	1	sets lamp
0	0	1	0	2	resets lamp
0	0	1	1	2	sets lamp
0	1	0	0	3	resets lamp
0	1	0	1	3	sets lamp
0	1	1	0	4	resets lamp
0	1	1	1	4	sets lamp
1	0	0	0	5	resets lamp
1	0	0	1	5	sets lamp
1	0	1	0	6	resets lamp
1	0	1	1	6	sets lamp
1	1	0	0	7	resets lamp
1	1	0	1	7	sets lamp
1	1	1	0	8	resets buzzer
1	1	1	1		sets buzzer

at least one of bits 7:4 must be non-zero

TABLE 12.15 KEYBOARD LAMP CONTROL

12.34 General Reset

A General Reset (GEN RES) to the Input/Output Coupler resets all commands and removes any outstanding Service Requests. The microprogram is allowed to cycle continually and reset all the keyboard lamps and the buzzer.

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